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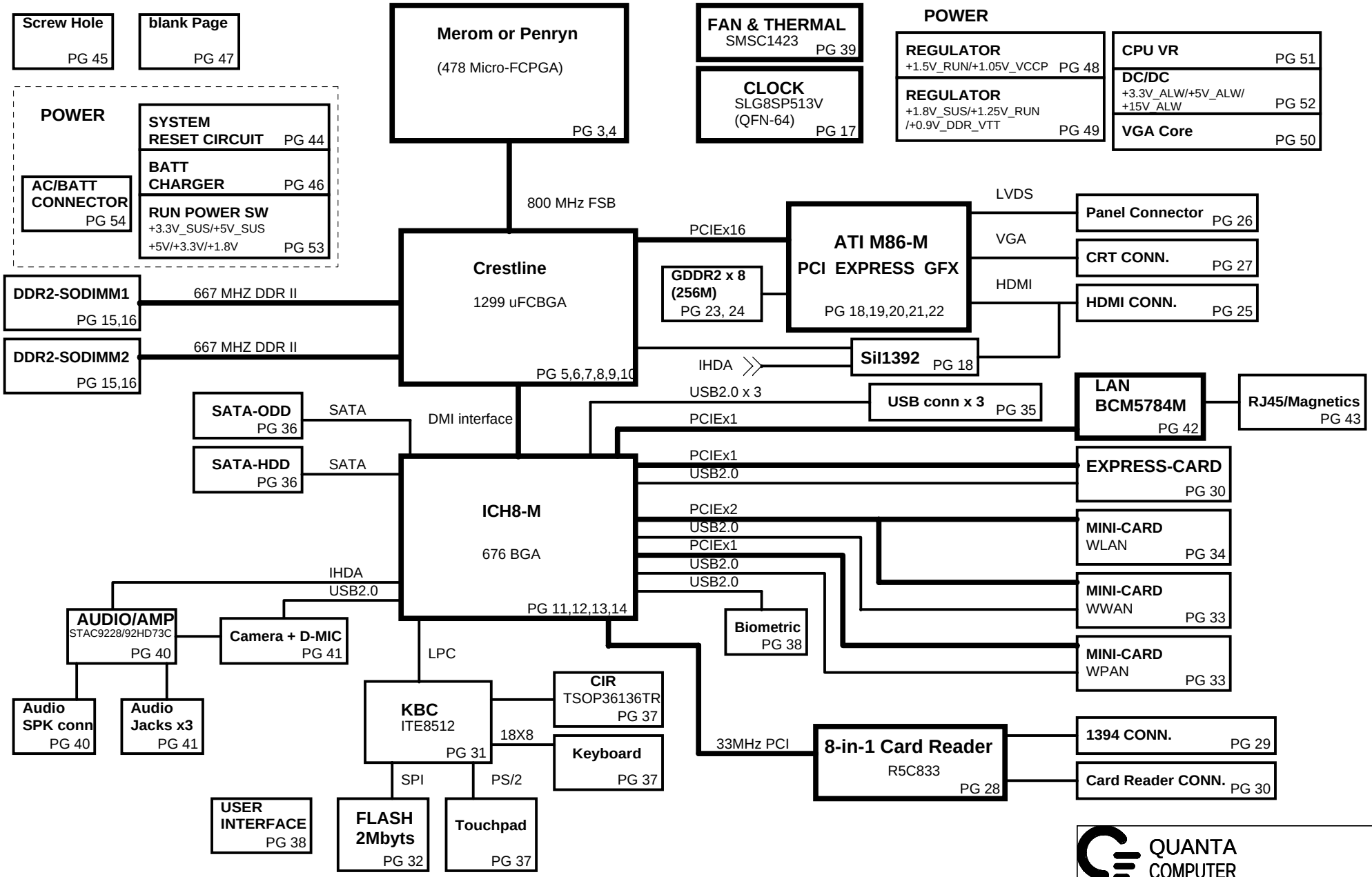
GM3(B) Pacino Intel Discrete & UMA Block Diagram

VER : 2A



QUANTA COMPUTER

Title	Schematic Block Diagram1	
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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,48,49,50,51,52,55	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,26,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,50,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,20,30,37,38,43,48,49,50,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,50,53,55	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,20,25,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	6,8,9,11,12,13,14,15,17,19,20,22,25,26,27,28,30,33,34,36,38,39,40,41,42,53,55	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	19,20,21,22,23,24,25,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,,53,55	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.25V_RUN	+1.25V	6,9,14,49,53	CALISTOGA/ICH8 POWER	1.25V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,37,48,55	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.5V	4,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	
+5V_ALW2	+5V	37,38.52,53	LED power source	LDO output	

GND PLANE	PAGE	DESCRIPTION
8731AGND	46	
AGND_0.9V	49	
AGND_DC/DC	52	
AGND_DC2	48	
AGND_DDR	49	
AGND_ISL6260	51	
GND	ALL	

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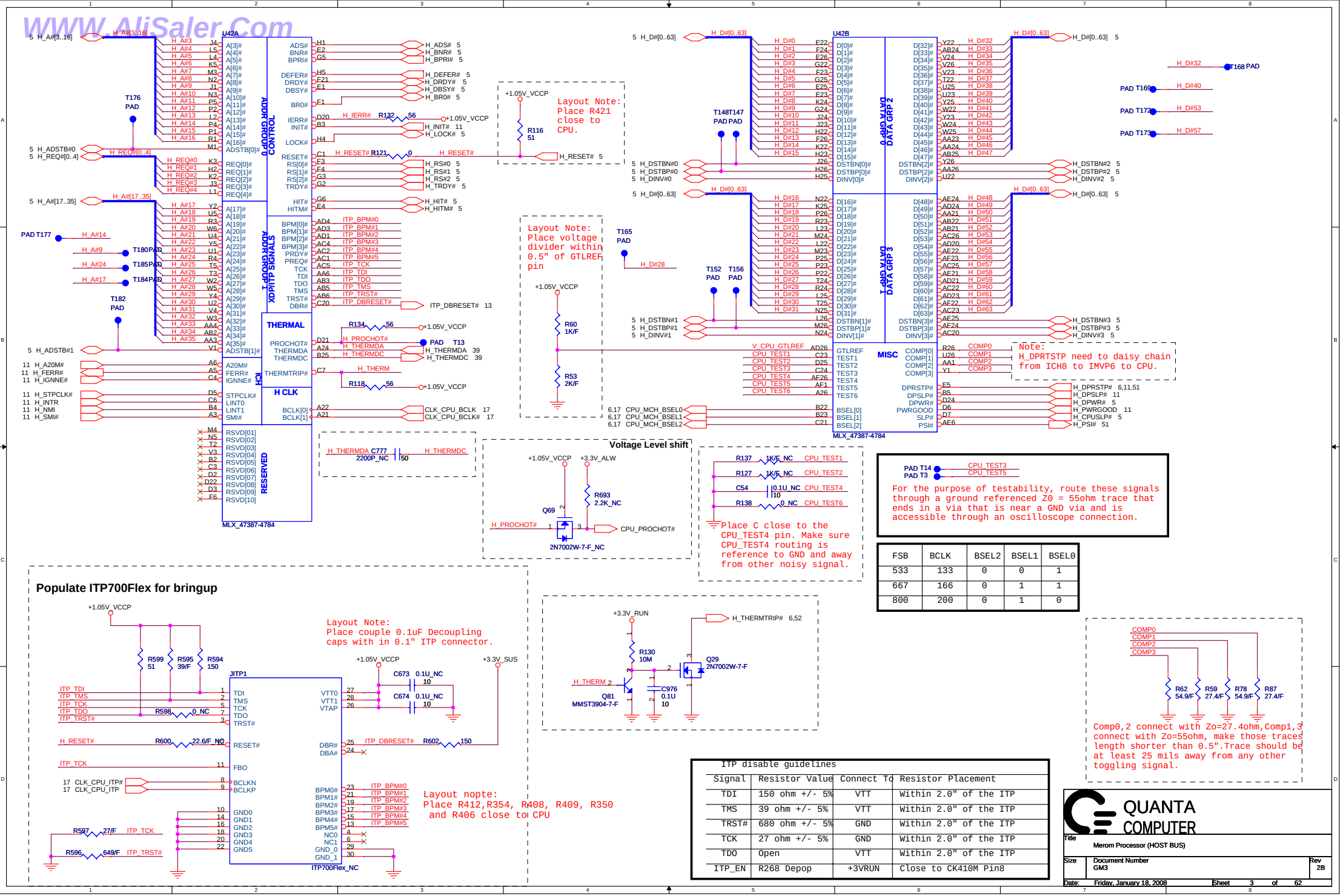

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 5%	GND	Within 2.0" of the ITP
TDO	Open	VTT	Within 2.0" of the ITP
ITP_EN	R268 Depop	+3VRUN	Close to CK410M Pin8

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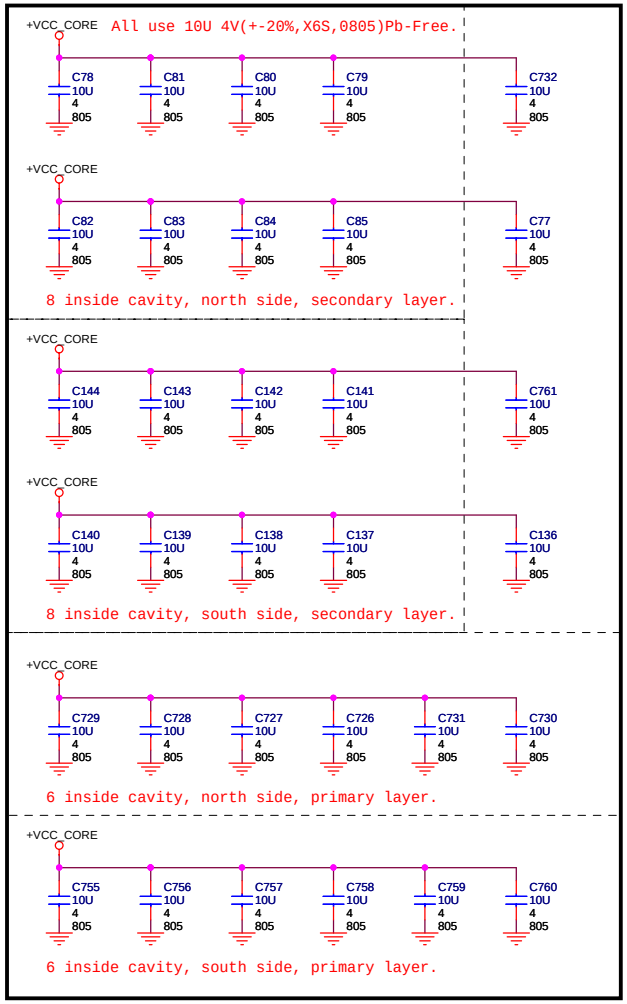

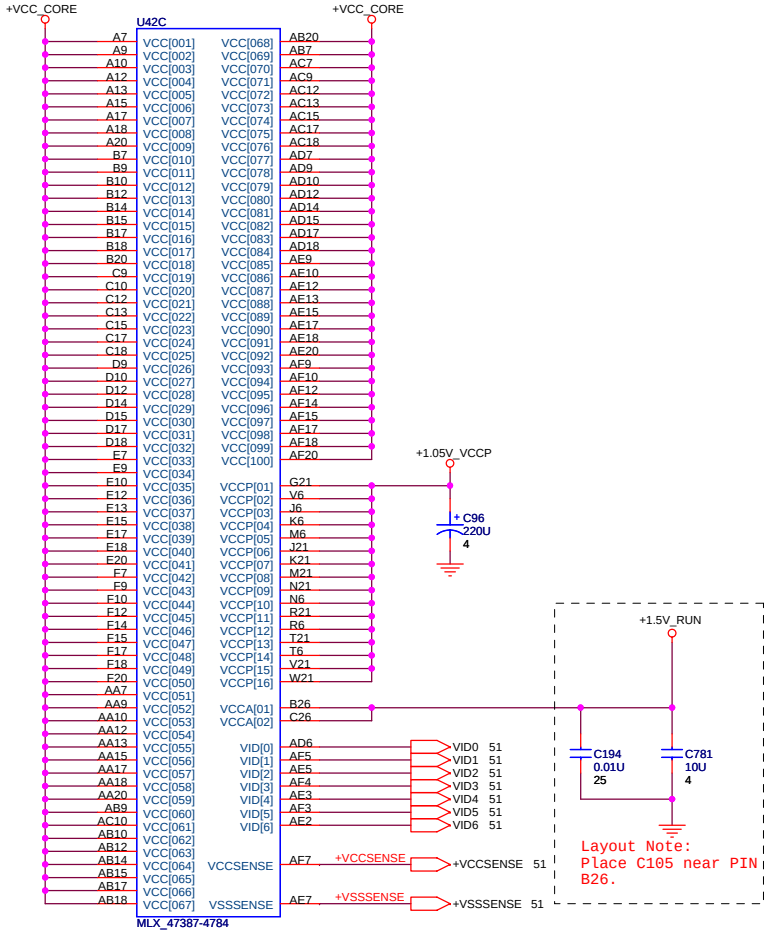

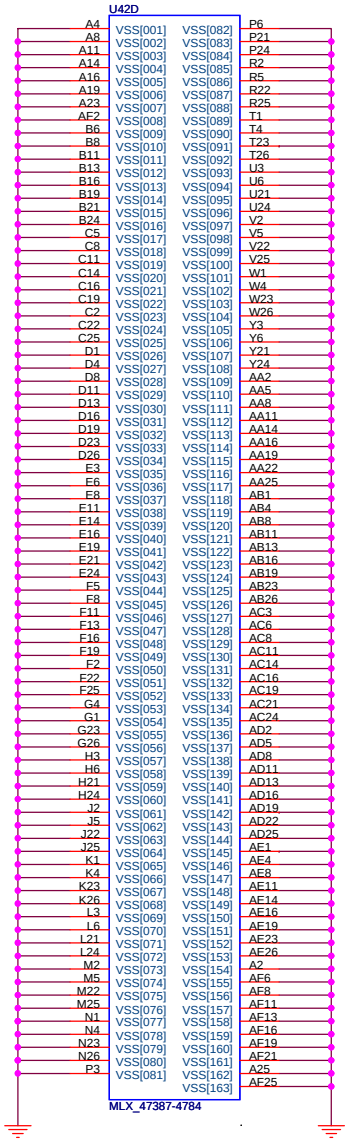

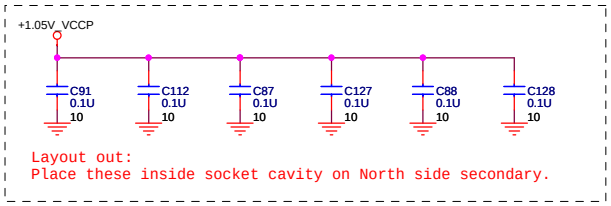

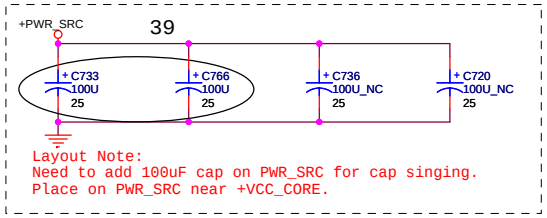

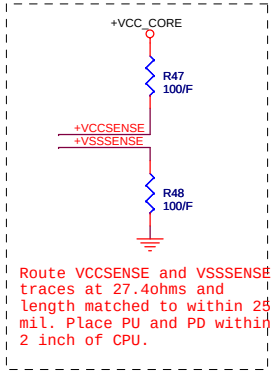

QUANTA COMPUTER

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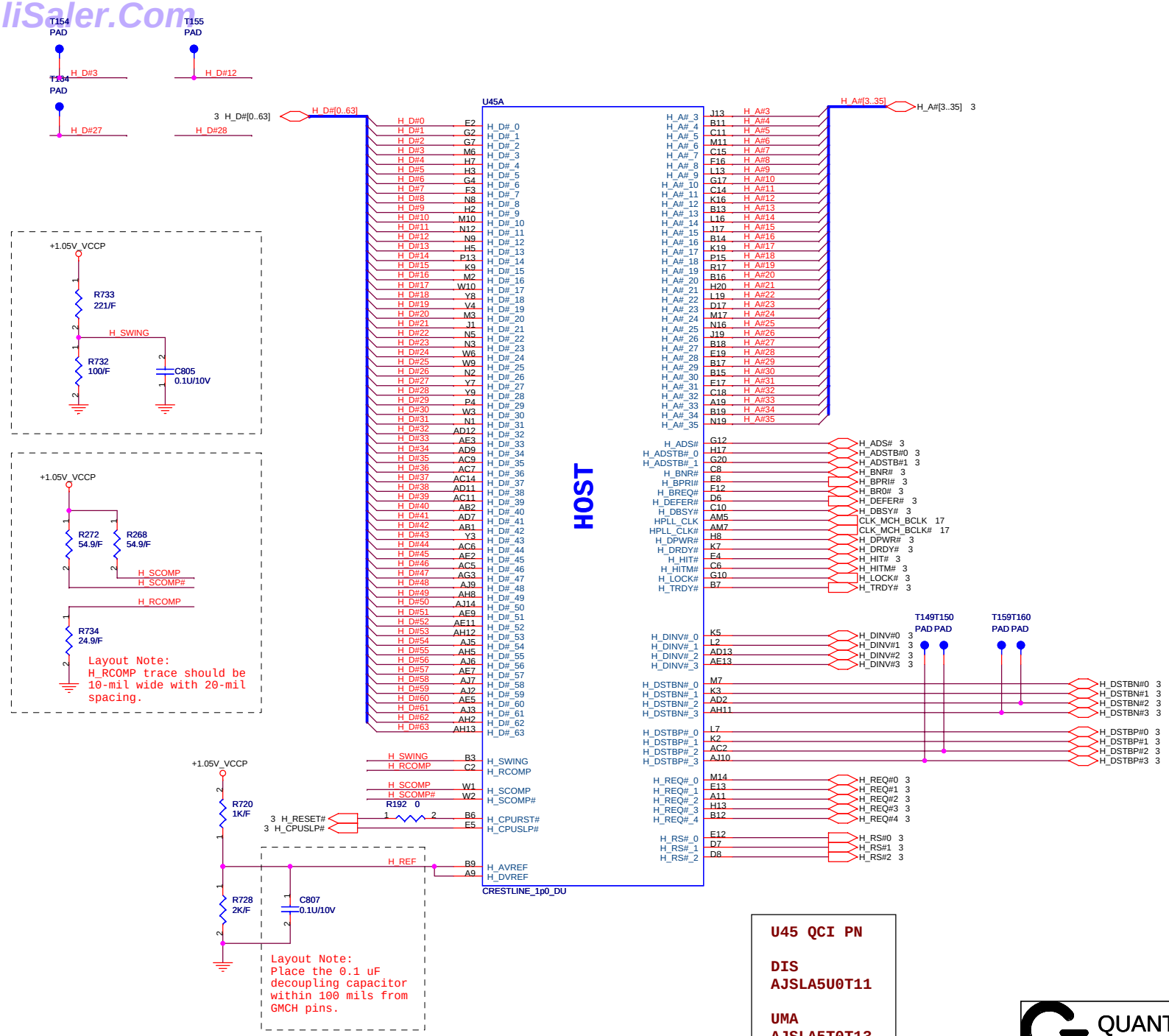

U45 QCI PN

DIS
AJSLA5U0T11

UMA
AJSLA5T0T13

QUANTA COMPUTER

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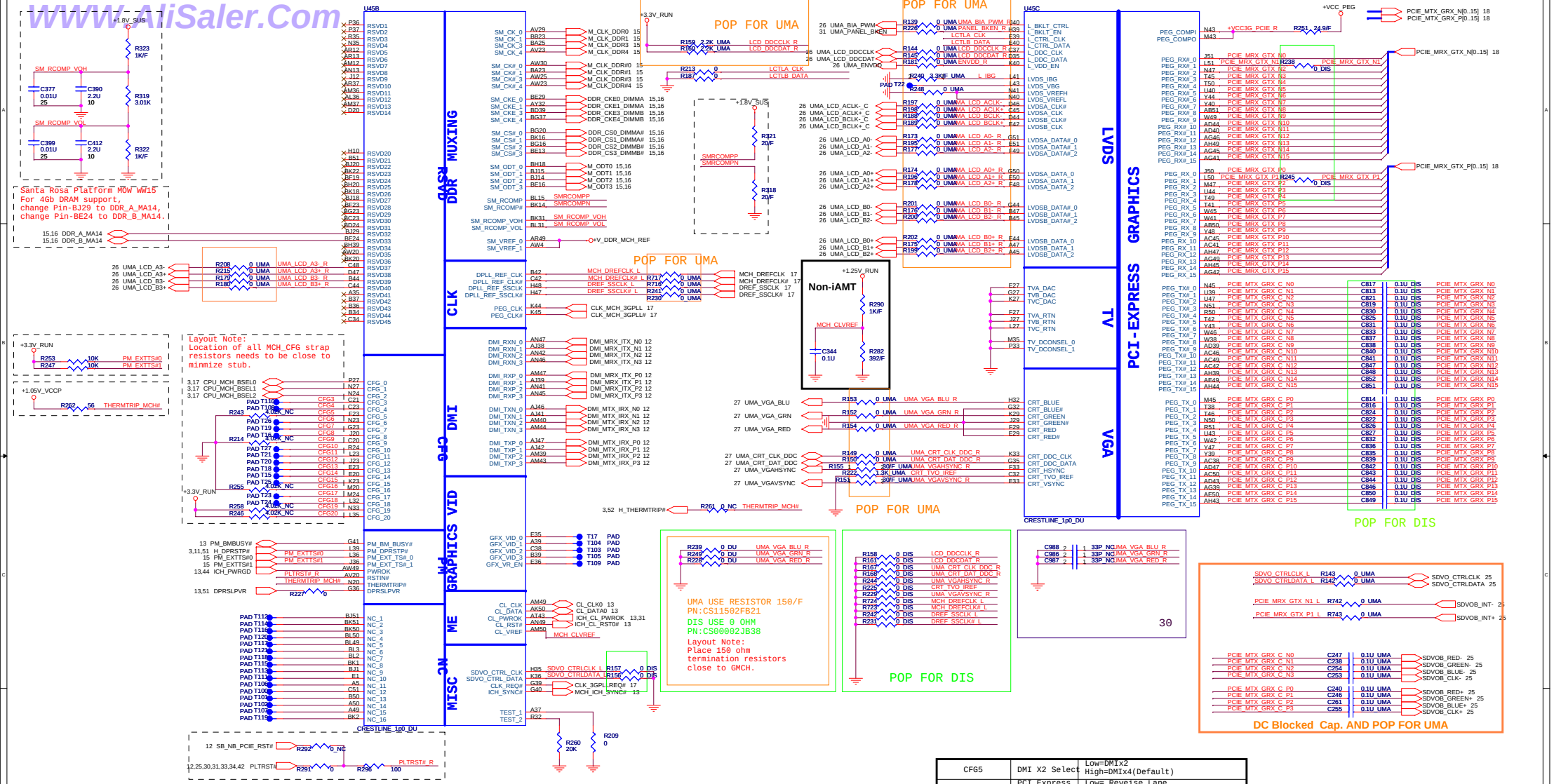

CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reveise Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present

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Title: Crestline (VGA,DMI)

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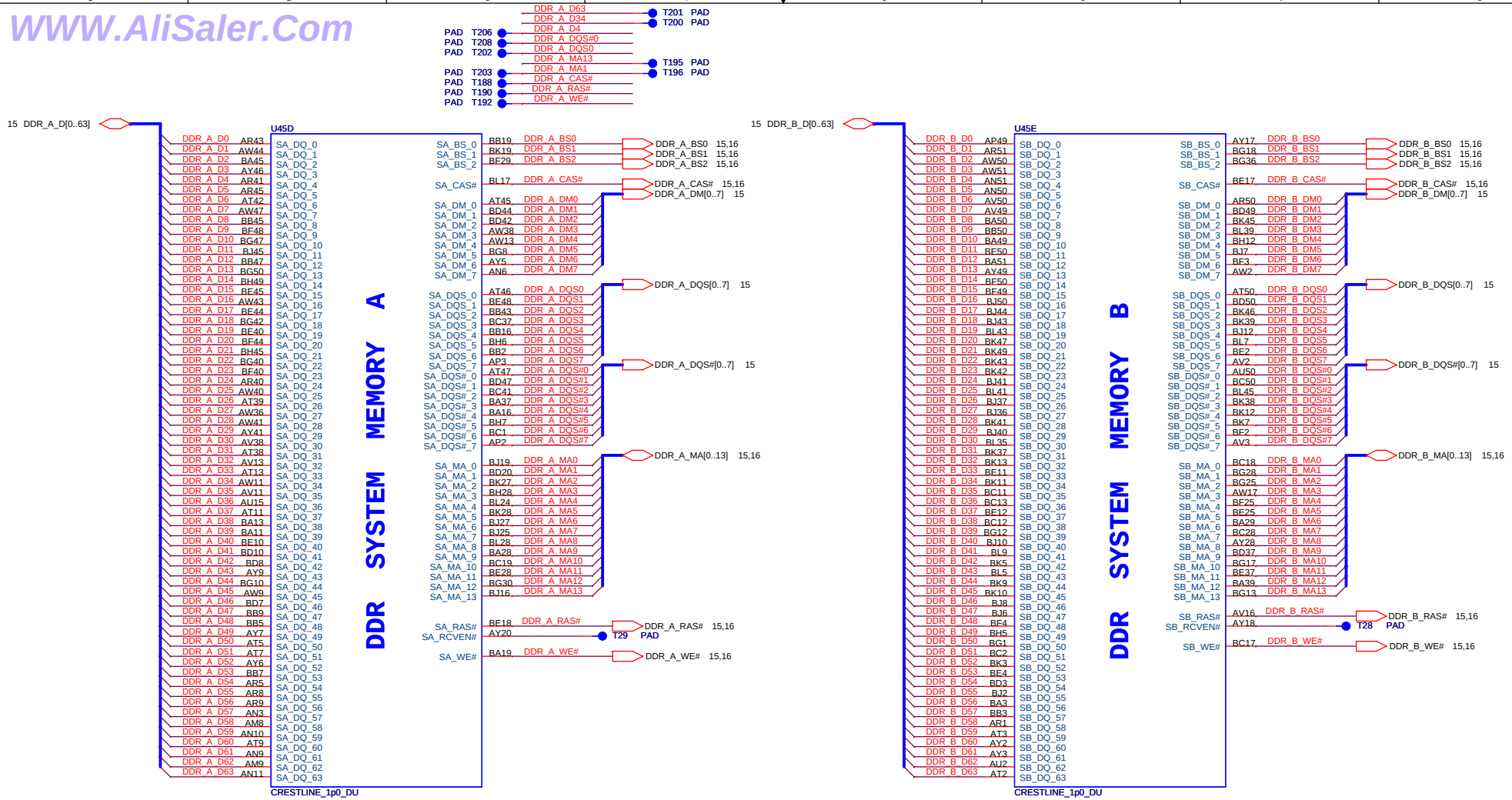

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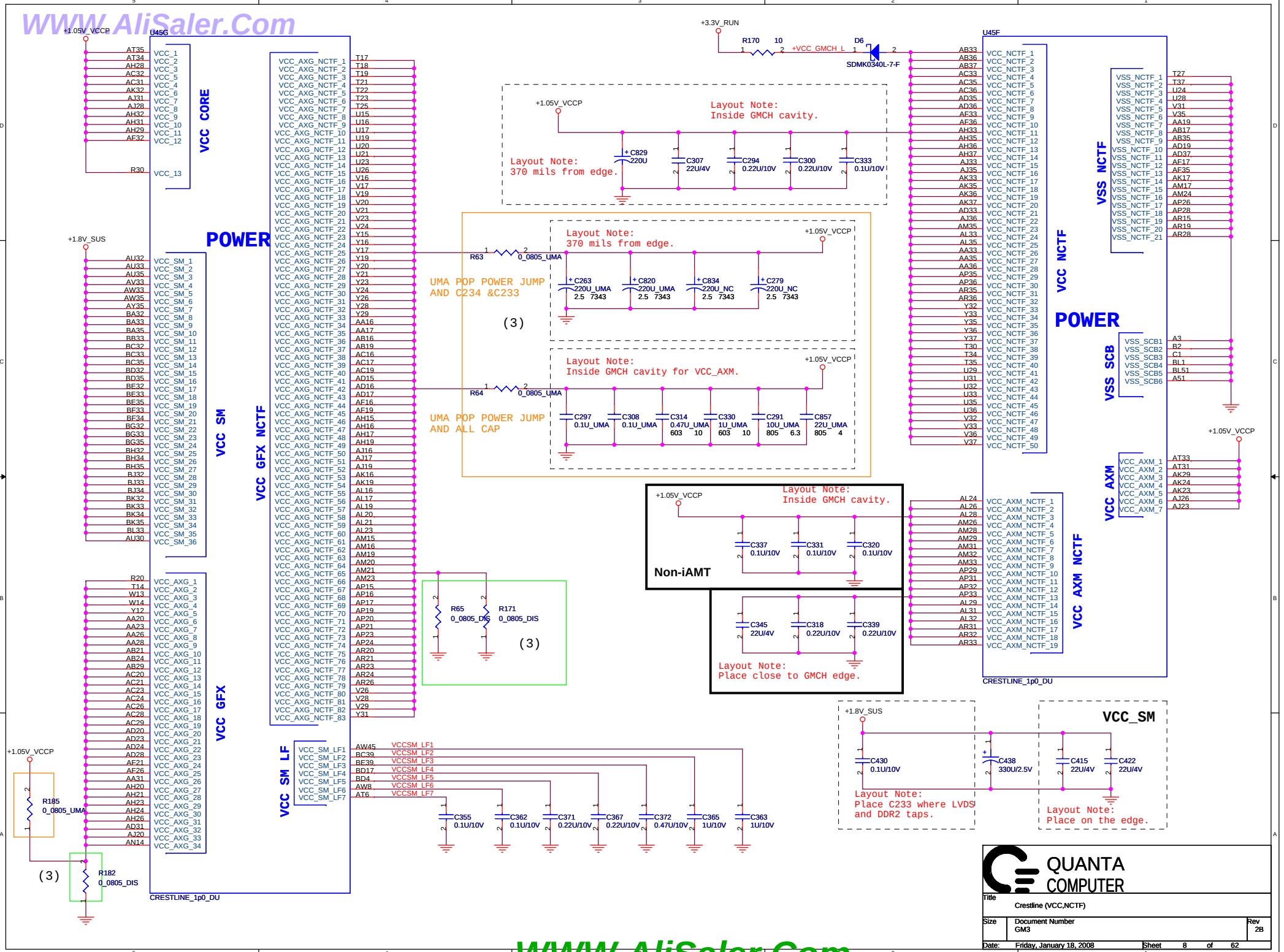

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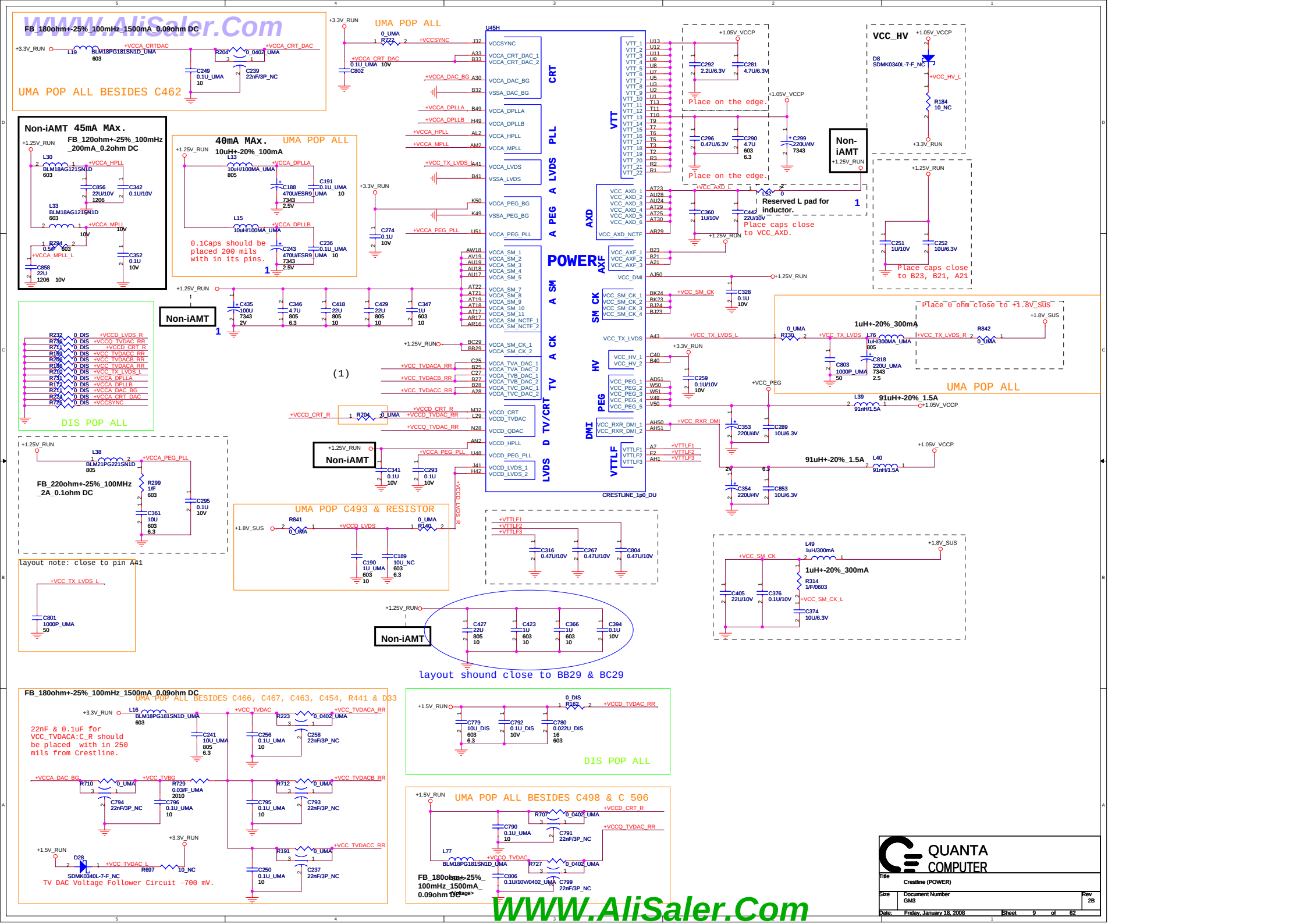
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FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC
UMA POP ALL BESIDES C462
UMA POP ALL
Non-iAMT 45mA MAx.
FB_120ohm+-25%_100mHz_200mA_0.2ohm DC
40mA MAx.
10uH+-20%_100mA
0.1Caps should be placed 200 mils with in its pins.
Non-iAMT
DIS POP ALL
FB_220ohm+-25%_100MHz_2A_0.1ohm DC
layout note: close to pin A41
UMA POP C493 & RESISTOR
POWER
CRESTLINE_1p0_DU
Place on the edge.
Reserved L pad for inductor.
Place caps close to VCC_AXD.
Place caps close to B23, B21, A21
VCC_HV
Place 0 ohm close to +1.8V_SUS
1uH+-20%_300mA
91uH+-20%_1.5A
layout shound close to BB29 & BC29
FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC
UMA POP ALL BESIDES C466, C467, C463, C454, R441 & D33
22nF & 0.1uF for VCC_TVDACA:C_R should be placed with in 250 mils from Crestline.
TV DAC Voltage Follower Circuit -700 mV.
DIS POP ALL
UMA POP ALL BESIDES C498 & C 506
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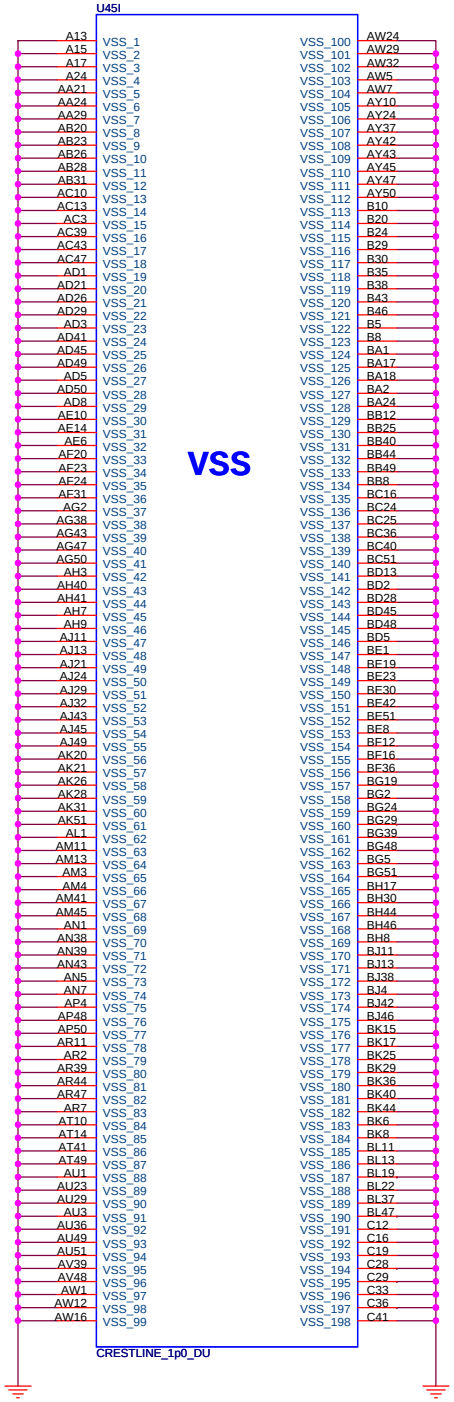

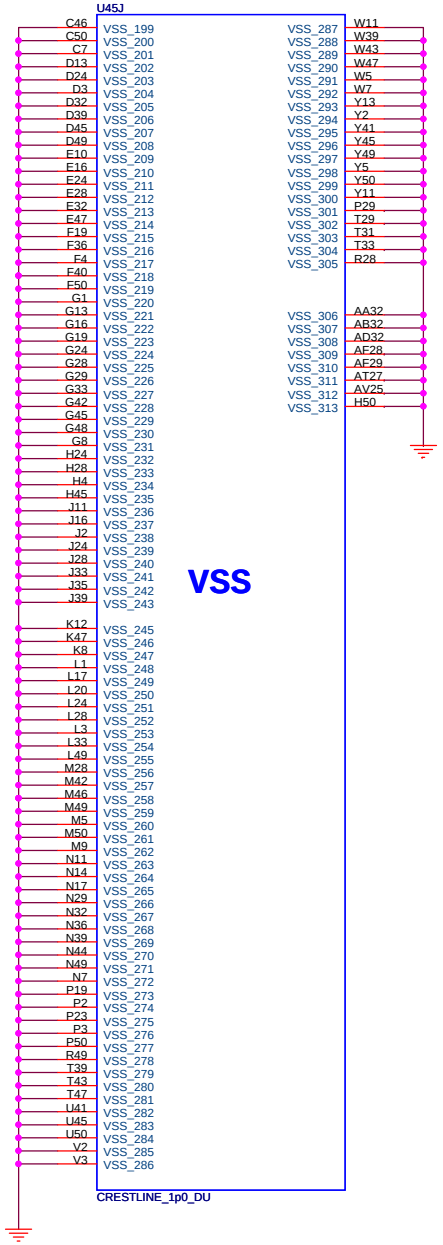

QUANTA COMPUTER

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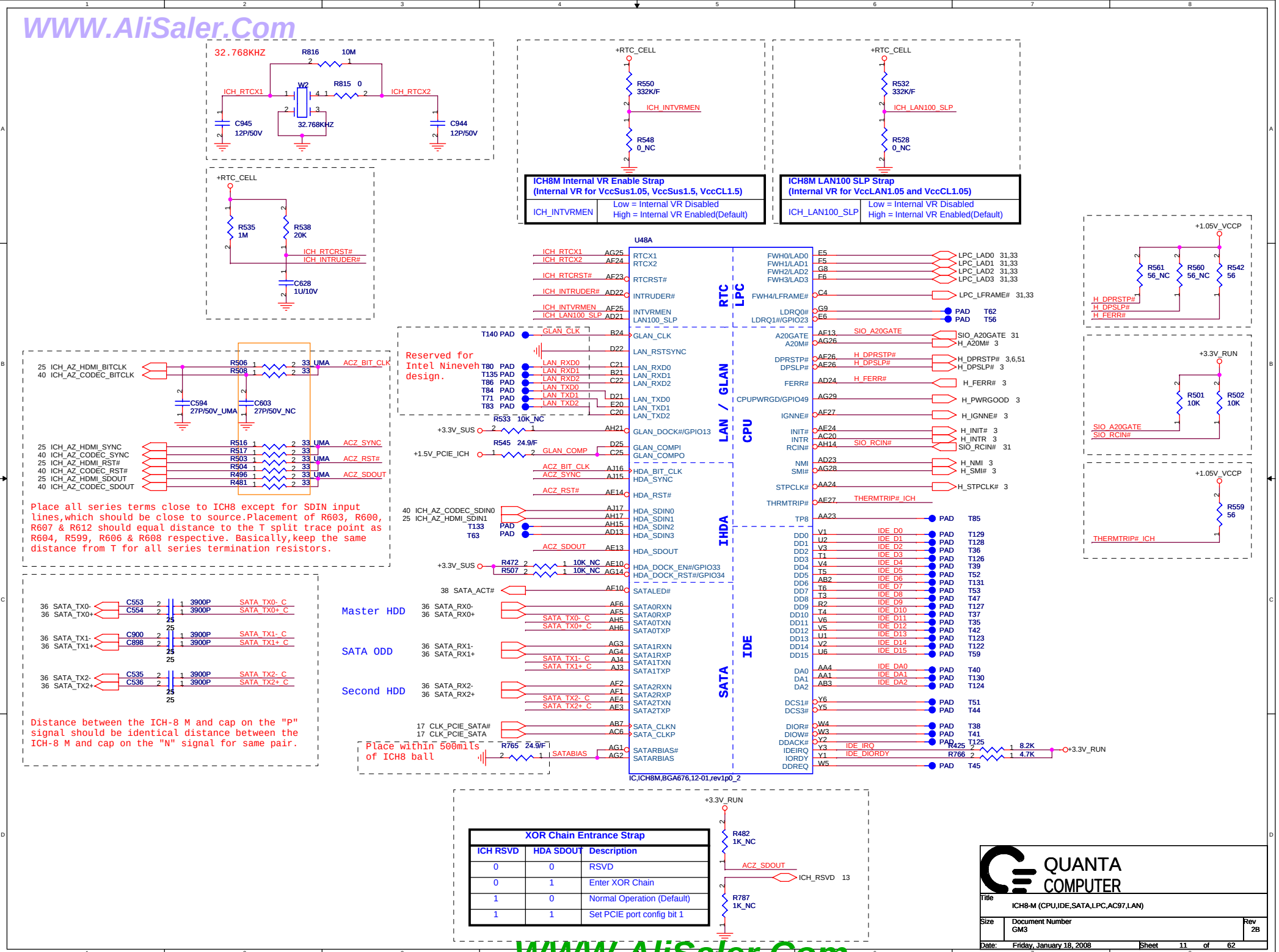

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Place TX DC blocking caps close ICH8.

33 PCIE_TX1- C953 0.1U PCIE_TXN1_C
33 PCIE_TX1+ C955 0.1U PCIE_TXP1_C
34 PCIE_TX2- C951 0.1U PCIE_TXN2_C
34 PCIE_TX2+ C952 0.1U PCIE_TXP2_C
33 PCIE_TX3- C949 0.1U PCIE_TXN3_C
33 PCIE_TX3+ C950 0.1U PCIE_TXP3_C
30 PCIE_TX4- C948 0.1U PCIE_TXN4_C
30 PCIE_TX4+ C947 0.1U PCIE_TXP4_C
42 PCIE_TX6-/GLAN_TX- C946 0.1U GLAN_TXN_C
42 PCIE_TX6+/GLAN_TX+ C954 0.1U GLAN_TXP_C

U48D — PCI-Express Direct Media Interface

MiniWWAN: 33 PCIE_RX1- / 33 PCIE_RX1+ — PERN1 P27, PERP1 P26, PETN1 N29, PETP1 N28
MiniWLAN: 34 PCIE_RX2- / 34 PCIE_RX2+ — PERN2 M27, PERP2 M26, PETN2 L29, PETP2 L28
MiniWPAN: 33 PCIE_RX3- / 33 PCIE_RX3+ — PERN3 K27, PERP3 K26, PETN3 J29, PETP3 J28
Express Card: 30 PCIE_RX4- / 30 PCIE_RX4+ — PERN4 H27, PERP4 H26, PETN4 G29, PETP4 G28
PERN5 F27, PERP5 E26, PETN5 E29, PETP5 E28
Giga Bit LOM: 42 PCIE_RX6-/GLAN_RX- / 42 PCIE_RX6+/GLAN_RX+ — PERN6/GLAN_RXN D27, PERP6/GLAN_RXP D26, PETN6/GLAN_TXN C29, PETP6/GLAN_TXP C28

DMI0RXN V27, DMI0RXP V26, DMI0TXN U29, DMI0TXP U28 — DMI_MTX_IRX_N0 6, DMI_MTX_IRX_P0 6, DMI_MRX_ITX_N0 6, DMI_MRX_ITX_P0 6
DMI1RXN Y27, DMI1RXP Y26, DMI1TXN W29, DMI1TXP W28 — DMI_MTX_IRX_N1 6, DMI_MTX_IRX_P1 6, DMI_MRX_ITX_N1 6, DMI_MRX_ITX_P1 6
DMI2RXN AB26, DMI2RXP AB25, DMI2TXN AA29, DMI2TXP AA28 — DMI_MTX_IRX_N2 6, DMI_MTX_IRX_P2 6, DMI_MRX_ITX_N2 6, DMI_MRX_ITX_P2 6
DMI3RXN AD27, DMI3RXP AD26, DMI3TXN AC29, DMI3TXP AC28 — DMI_MTX_IRX_N3 6, DMI_MTX_IRX_P3 6, DMI_MRX_ITX_N3 6, DMI_MRX_ITX_P3 6
DMI_CLKN T26, DMI_CLKP T25 — CLK_PCIE_ICH# 17, CLK_PCIE_ICH 17
DMI_ZCOMP Y23, DMI_IRCOMP Y24 — DMI_COMP — R529 24.9/F — +1.5V_PCIE_ICH

Place within 500mils of ICH8

SPI: SPI_CLK C23, SPI_CS0# B23, SPI_CS1# E22, SPI_MOSI D23, SPI_MISO F21
USB: OC0# AJ19, OC1#/GPIO40 AG16, OC2#/GPIO41 AG15, OC3#/GPIO42 AE15, OC4#/GPIO43 AE15, OC5#/GPIO29 AG17, OC6#/GPIO30 AD12, OC7#/GPIO31 AJ18, OC8# AD14, OC9# AH18

35 USB_OC0_1# — USB_OC0_1#
54 USB_OC2_3# — USB_OC2_3#
35 USB_OC8# — USB_OC8#

USB port pins: G3, G2, H5, H4, H2, H1, J3, J2, K5, K4, K2, K1, L3, L2, M5, M4, M2, M1, N3, N2
ICH_USBP0- 35, ICH_USBP0+ 35, ICH_USBP1- 35, ICH_USBP1+ 35, ICH_USBP2- 54, ICH_USBP2+ 54, ICH_USBP3- 54, ICH_USBP3+ 54, ICH_USBP4- 41, ICH_USBP4+ 41, ICH_USBP5- 33, ICH_USBP5+ 33, ICH_USBP6- 33, ICH_USBP6+ 33, ICH_USBP7- 30, ICH_USBP7+ 30, ICH_USBP8- 35, ICH_USBP8+ 35, ICH_USBP9- 38, ICH_USBP9+ 38

Side pair Top / left
Side pair bottom / left
Side pair top/right(DB)
Side pair Bot right(DB)
Camera
Mini Card (WWAN)
Mini Card (WPAN)
Express Card
left side signal USB port
Biometric

USBRBIAS# F2, USBRBIAS F3 — USBRBIAS — R763 22.6/F

Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

ICH_SPI_CS1_R
PCI_GNT0#
R451 1K_NC, R546 1K_NC

Boot BIOS Strap

		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

PCI Pullups

RP42: PCI_FRAME#, PCI_STOP#, PCI_DEVSEL#, PCI_REQ1# — PCI_TRDY#, PCI_PIRQD#, PCI_PIRQB#, PCI_SERR# — +3.3V_RUN
RP40: PCI_IRDY#, PCI_PERR#, PCI_PLOCK#, PCI_PIRQB# — PCI_PIRQA#, ICH_IRQH_GPIO5, PCI_PIRQC#, PCI_REQ0# — +3.3V_RUN

WWAN Noise - ICH improvements

OC6# C918 0.1U_NC, OC4# C915 0.1U_NC, OC5# C916 0.1U_NC, OC7# C917 0.1U_NC, USB_OC8# C922 0.1U_NC, USB_OC2_3# C923 0.1U_NC, USB_OC0_1# C924 0.1U_NC, OC9# C925 0.1U_NC

Non-iAMT (19)

RP49 10KX8: OC6#, OC4#, OC5#, OC7# — USB_OC8#, USB_OC2_3#, USB_OC0_1#, OC9# — +3.3V_SUS

SB_WPAN_PCIE_RST# R468 20K
SB_WWAN_PCIE_RST# R791 20K
SB_WLAN_PCIE_RST# R467 20K
SB_LOM_PCIE_RST# R477 20K
SB_NB_PCIE_RST# R495 20K

BIOS should not enable the internal GPIO pull up resistor.

28 PCI_AD[0..31]

U48B — PCI

PCI_AD0 D20, PCI_AD1 E19, PCI_AD2 D19, PCI_AD3 A20, PCI_AD4 D17, PCI_AD5 A21, PCI_AD6 A19, PCI_AD7 C19, PCI_AD8 A18, PCI_AD9 B16, PCI_AD10 A12, PCI_AD11 E16, PCI_AD12 A14, PCI_AD13 G16, PCI_AD14 A15, PCI_AD15 B6, PCI_AD16 C11, PCI_AD17 A9, PCI_AD18 D11, PCI_AD19 B12, PCI_AD20 C12, PCI_AD21 D10, PCI_AD22 C7, PCI_AD23 F13, PCI_AD24 E11, PCI_AD25 E13, PCI_AD26 E12, PCI_AD27 D8, PCI_AD28 A6, PCI_AD29 E8, PCI_AD30 D6, PCI_AD31 A3

REQ0# A4 PCI_REQ0# — PCI_REQ0# 28
GNT0# D7 PCI_GNT0# — PCI_GNT0# 28
REQ1#/GPIO50 E18 PCI_REQ1# — PAD T65
GNT1#/GPIO51 C18 PCI_GNT1# — PAD T75
REQ2#/GPIO52 B19 SB_WWAN_PCIE_RST# — SB_WWAN_PCIE_RST# 33
GNT2#/GPIO53 E18 PCI_GNT2# — PAD T64
REQ3#/GPIO54 A11 SB_LOM_PCIE_RST# — SB_LOM_PCIE_RST# 42
GNT3#/GPIO55 C10 PCI_GNT3# — PAD T61
C/BE0# C17 — PCI_C_BE0# 28
C/BE1# E15 — PCI_C_BE1# 28
C/BE2# E16 — PCI_C_BE2# 28
C/BE3# E17 — PCI_C_BE3# 28
IRDY# C8 PCI_IRDY# — PCI_IRDY# 28
PAR D9 — PCI_PAR 28
PCIRST# G6 PCI_RST# G
DEVSEL# D16 PCI_DEVSEL# — PCI_DEVSEL# 28
PERR# A7 PCI_PERR# — PCI_PERR# 28
PLOCK# B7 PCI_PLOCK# — PCI_PLOCK#
SERR# E10 PCI_SERR# — PCI_SERR# 28
STOP# C16 PCI_STOP# — PCI_STOP# 28
TRDY# C9 PCI_TRDY# — PCI_TRDY# 28
FRAME# A17 PCI_FRAME# — PCI_FRAME# 28
PLTRST# AG24 PCI_PLTRST#
PCICLK B10 CLK_PCI_ICH — CLK_PCI_ICH 17
PME# G7 — ICH_PME# 28,31

Interrupt I/F
PIRQA# F9 PCI_PIRQA# — T55 PAD
PIRQB# B5 PCI_PIRQB# — 28 PCI_PIRQB#
PIRQC# C5 PCI_PIRQC# — 28 PCI_PIRQC#
PIRQD# A10 PCI_PIRQD# — T132 PAD
PIRQE#/GPIO2 E8 SB_WPAN_PCIE_RST# — SB_WPAN_PCIE_RST# 33
PIRQF#/GPIO3 G11 SB_WLAN_PCIE_RST# — SB_WLAN_PCIE_RST# 34
PIRQG#/GPIO4 E12 SB_NB_PCIE_RST# — SB_NB_PCIE_RST# 6
PIRQH#/GPIO5 B3 ICH_IRQH_GPIO5 — PAD T49

PCI_GNT3# — R474 1K_NC

A16 away override strap.

SB_NB_PCIE_RST#	Low = A16 swap override enabled. High = Default.

T210 PAD — PCI_AD15 — PAD T209
T213 PAD — PCI_AD2 — PAD T214
T215 PAD — PCI_AD3 — PAD T216
T217 PAD — PCI_AD0 — PAD T218
T219 PAD — PCI_AD2 — PAD T220
T221 PAD — PCI_AD21 — PAD T222
T223 PAD — PCI_AD17 — PAD T224
T225 PAD — PCI_AD16 — PAD T226
T229 PAD — PCI_IRDY# — PAD T230
T234 PAD — PCI_TRDY# — PAD T233
T228 PAD — PCI_FRAME# — PAD T227
T231 PAD — PCI_STOP# — PAD T232
T235 PAD — PCI_DEVSEL# — PAD T236
T237 PAD — PCI_GNT0# — PAD T238
PCI_REQ0# — PAD T239

CLK_PCI_ICH — R772 10_NC — C907 8.2P_NC

Reserved for EMI.Place resister and cap close to ICH.

Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

C887 0.047U — +3.3V_SUS — U47 — PCI_RST# G — PCI_RST# 28 — TC7SZ32FU(T5L,F,T)
C958 0.047U — +3.3V_SUS — U50 — PCI_PLTRST# — PLTRST# 6,25,30,31,33,34,42 — TC7SZ32FU(T5L,F,T)

QUANTA COMPUTER

Title	ICH8-M (USB,DMI,PCIE,PCI)	
Size	Document Number GM3	Rev 2B
Date: Friday, January 18, 2008	Sheet 12 of 62	

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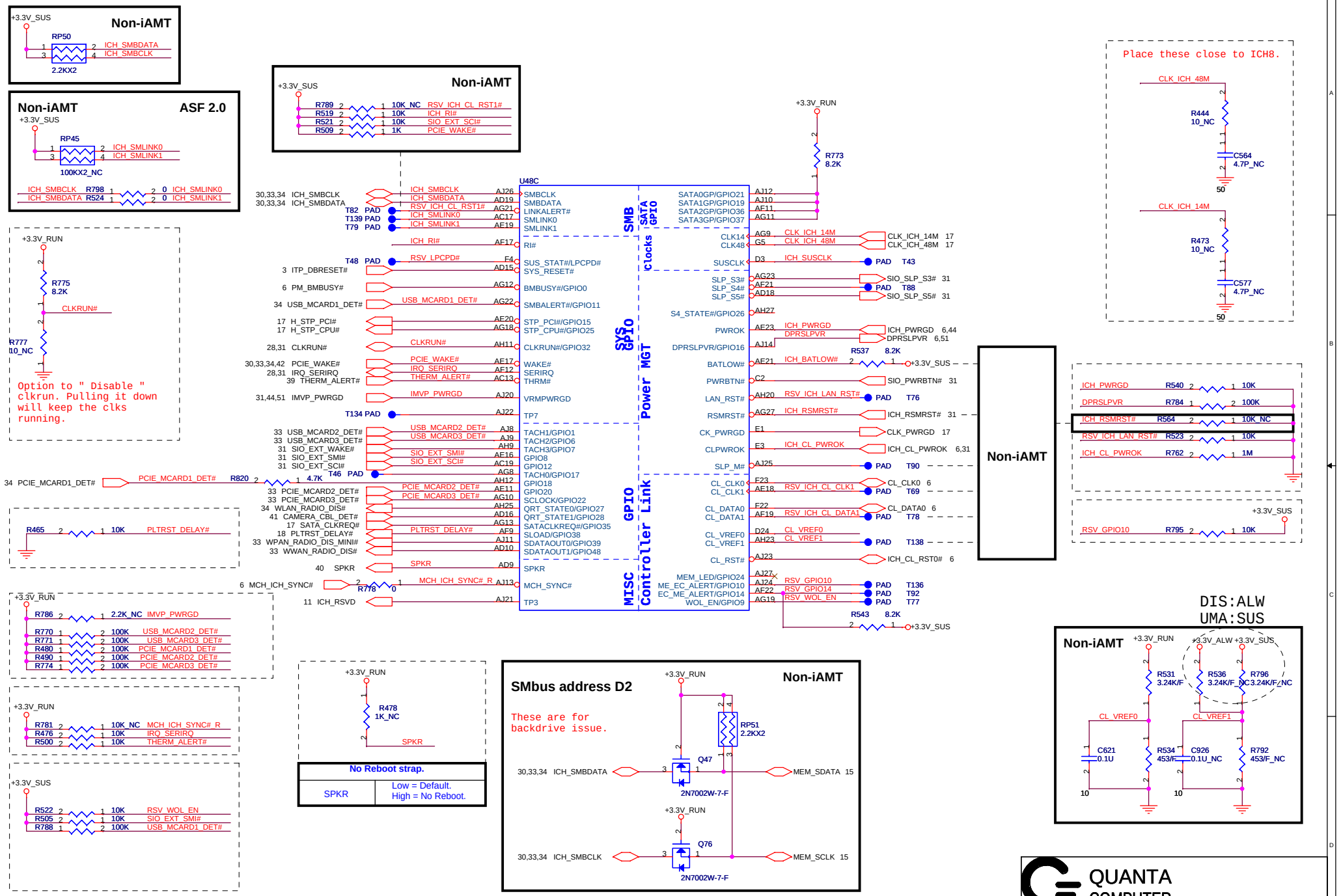

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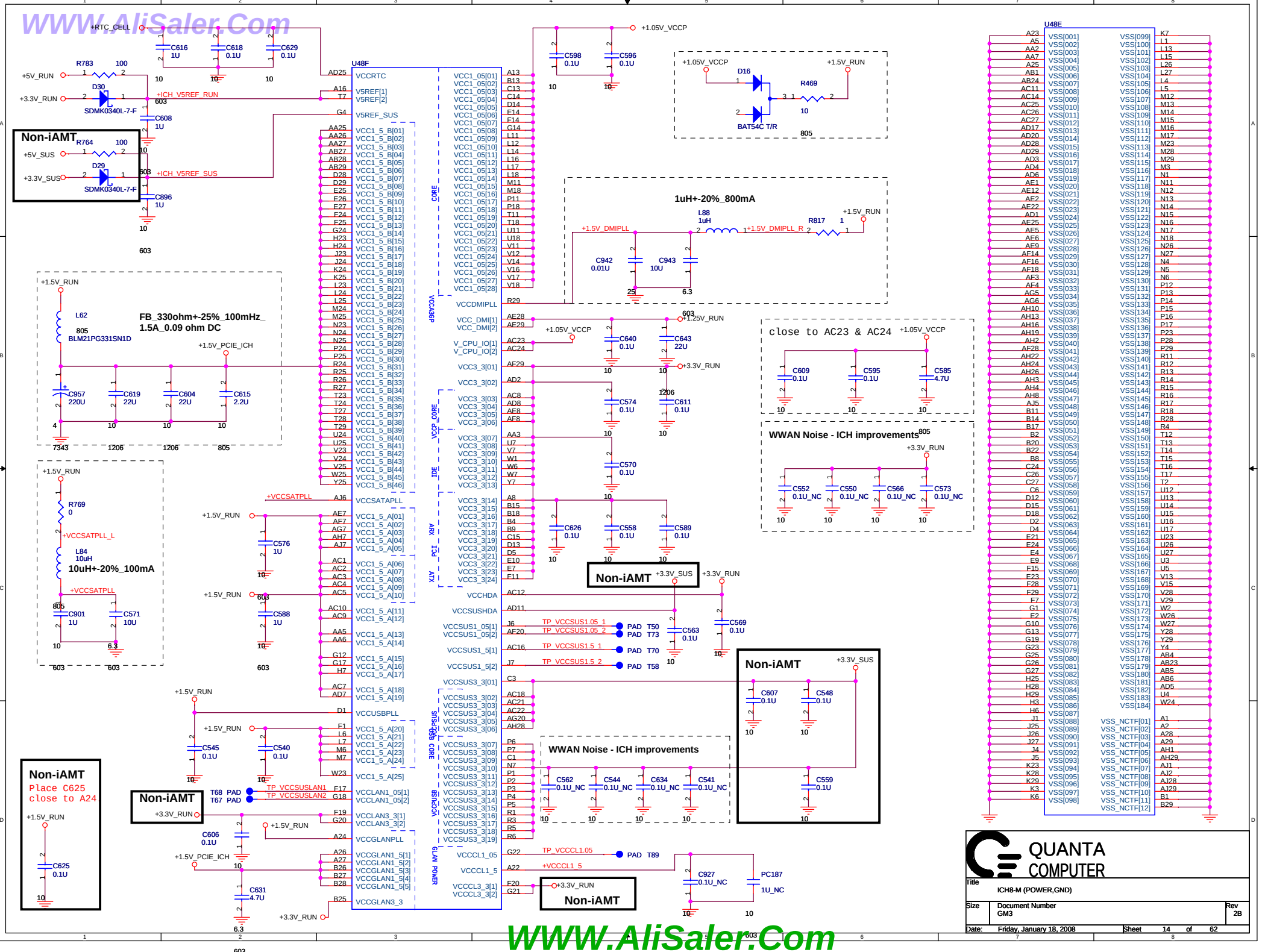

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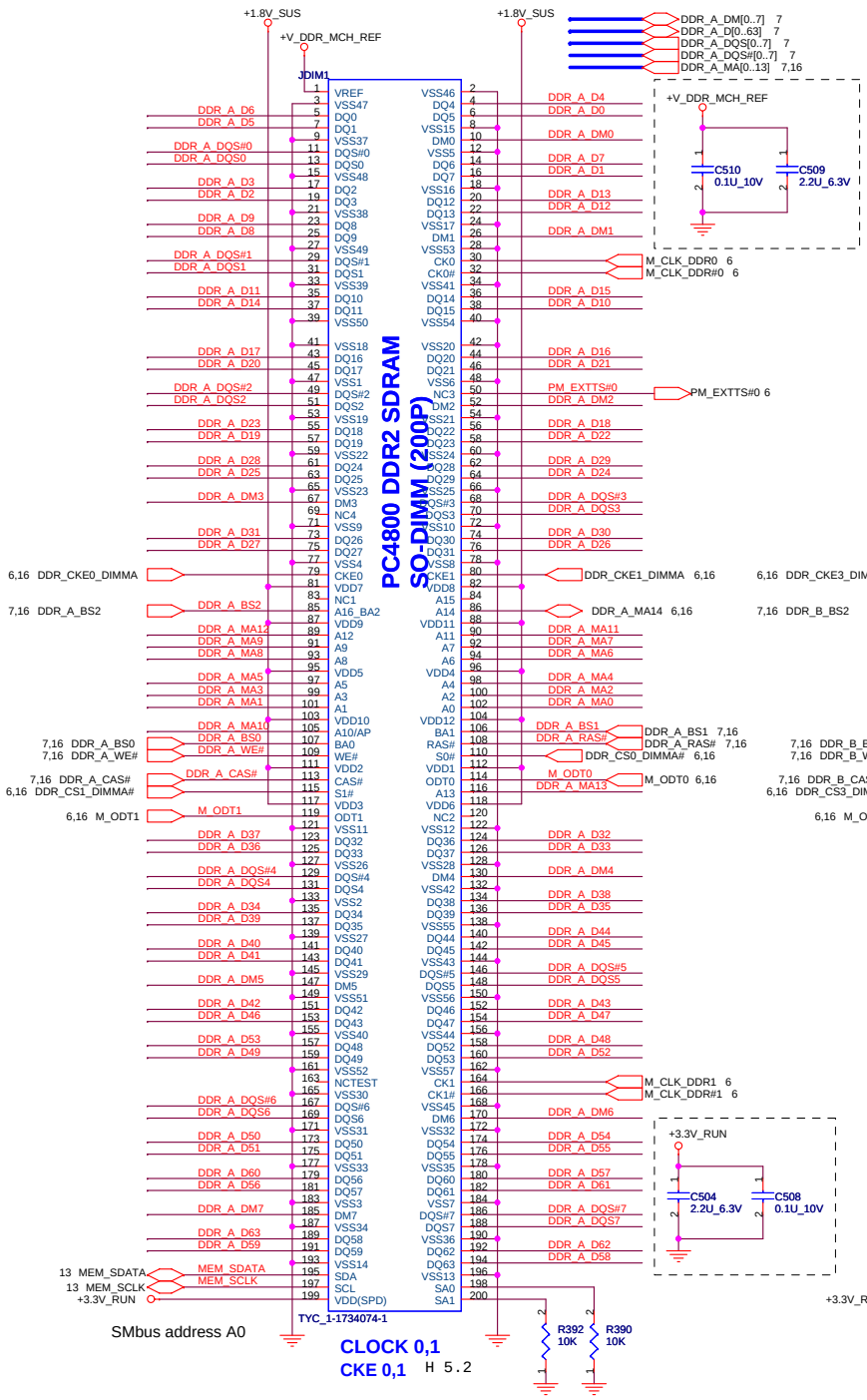
MASTER



SLAVE

QUANTA COMPUTER

Title	DDR2_SO-DIMM (200P) X 2
Size	Document Number GM3
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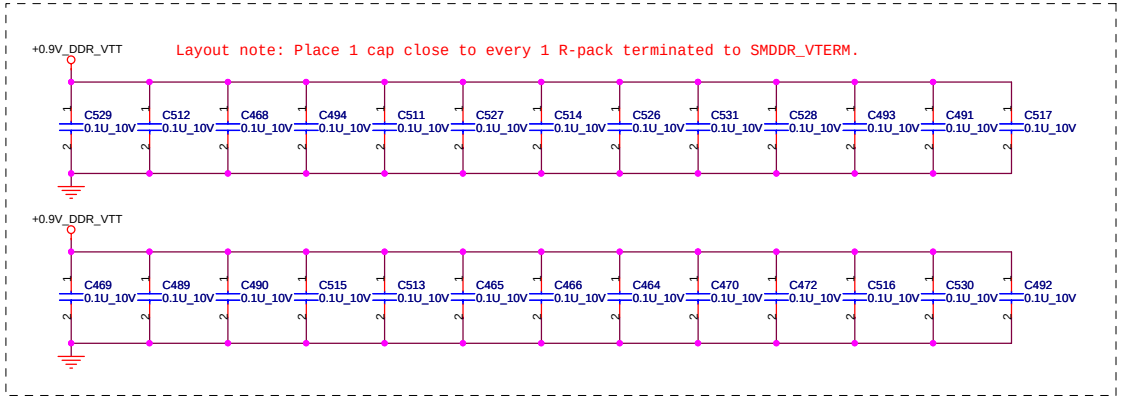

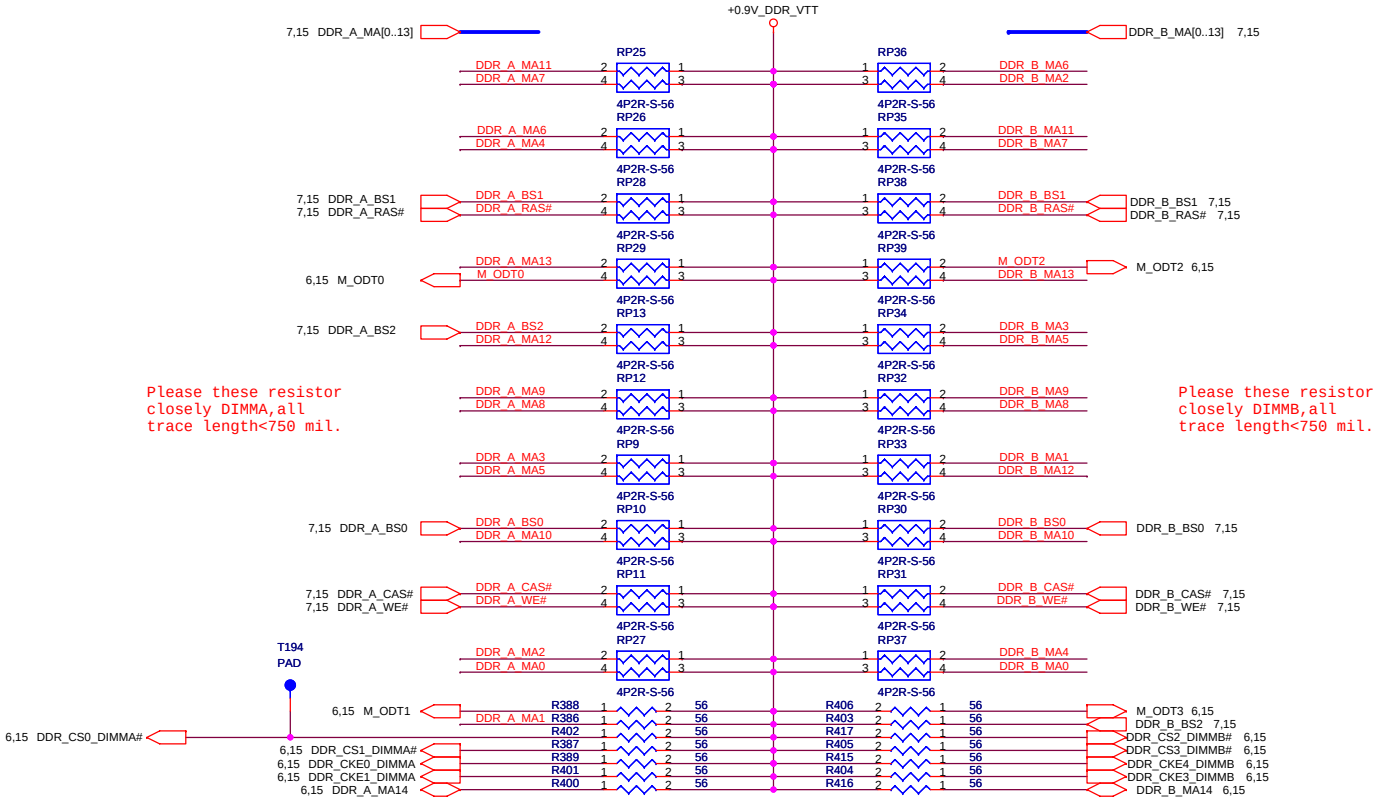

QUANTA COMPUTER

Title	DDR2 RES. ARRAY	
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Add capacitor pads for improving WWAN.

C457 27P CLK_ICH_48M
C440 27P_NC CLK_ICH_14M
C431 27P_NC CLK_PCI_8512
C432 27P_NC CLK_PCI_PCCARD
C439 27P_NC CLK_PCI_ICH

CLK_XTAL_IN — Y2 14.318MHZ — CLK_XTAL_OUT
C437 33P, C443 33P

14.318MHz

U19

CK505
QFN64

SLG8SP513V

+CK_VDD_PCI, +CK_VDD_PLL3, +CK_VDD_48, +CK_VDD_SRC, +CK_VDD_MAIN

VDD_PCI, VDD_REF, VDD_PLL3, VDD_48, VDD_SRC, VDD_CPU, VDD_IO, GND, CR#_A/PCI-0, CR_B/PCI-1, TME/PCI-2, SRC5_EN/PCI-3, 27M_SEL/PCI-4, ITP_EN/PCIF-5, FSA/USB48, FSB/TEST_MODE, FSC/TEST_SEL/REF, RESET#, CK_PWRGD/PD#, XOUT, XIN, SDATA, SCLK

13 SATA_CLKREQ# — SATA_CLKREQ# R365 475
6 CLK_3GPLLREQ# — CLK_3GPLLREQ# R364 475/F
33 CLK_LPC_DEBUG — CLK_LPC_DEBUG R363 22_NC
28 CLK_PCI_PCCARD — CLK_PCI_PCCARD R354 33
31 CLK_PCI_8512 — CLK_PCI_8512 R353 33
12 CLK_PCI_ICH — CLK_PCI_ICH R350 33
13 CLK_ICH_48M — CLK_ICH_48M R375 33
3,6 CPU_MCH_BSEL0 — L55 BLM18SG260 R372 8.2K
3,6 CPU_MCH_BSEL1 — R374 8.2K
3,6 CPU_MCH_BSEL2 — R367 8.2K
13 CLK_ICH_14M — CLK_ICH_14M R366 33
13 CLK_PWRGD

SATA_CLKREQ# C, CLK_3GPLLREQ# C, PCI_PCCARD, PCI_SIO, 27M_SEL, PCI_ICH, FSA, FSB, FSC

CLK_XTAL_OUT, CLK_XTAL_IN, CLK_SDATA, CLK_SCLK

CLK_LPC_DEBUG FOR DEBUG
NEED POP RESISTOR

CPU-0 / CPU-0# — CPU_BCLK / CPU_BCLK# — RP5 0 — CLK_CPU_BCLK 3 / CLK_CPU_BCLK# 3
CPU-1 / CPU-1# — MCH_BCLK / MCH_BCLK# — RP7 0 — CLK_MCH_BCLK 5 / CLK_MCH_BCLK# 5
SRC-8/CPU_ITP / SRC-8#/CPU_ITP# — CPU_ITP / CPU_ITP# — RP17 0 — CLK_PCIE_MINI1 34 / CLK_PCIE_MINI1# 34
SRC-0/DOT96 / SRC-0#/DOT96# — DOT96_SSC / DOT96_SSC# — RP4 0 DIS — CLK_PCIE_VGA 18 / CLK_PCIE_VGA# 18
SRC-1/SE1 / SRC-1#/SE2 — 27M_SS / 27M_NSS — RP8 0 DIS — CLK_VGA_27M_SS 19 / CLK_VGA_27M_NSS 19
SRC-2/SATA / SRC-2#/SATA# — PCIE_SATA / PCIE_SATA# — RP16 0 — CLK_PCIE_SATA 11 / CLK_PCIE_SATA# 11
CR#_C/SRC-3 / CR#_D/SRC-3# — PCIE_MINI3 / PCIE_MINI3# — RP18 0 — CLK_PCIE_MINI3 33 / CLK_PCIE_MINI3# 33
SRC-4 / SRC-4# — MCH_3GPLL / MCH_3GPLL# — RP20 0 — CLK_MCH_3GPLL 6 / CLK_MCH_3GPLL# 6
PCI_STOP#/SRC-5 / CPU_STOP#/SRC5-5# — H_STP_PCI# 13 / H_STP_CPU# 13
SRC-6 / SRC-6# — PCIE_EXPCARD / PCIE_EXPCARD# — RP24 0 — CLK_PCIE_EXPCARD 30 / CLK_PCIE_EXPCARD# 30
CR#_F/SRC-7 / CR#_E/SRC-7# — MINI1CLK_REQ# C, CARD_CLK_REQ# C — R394 475/F, R395 475/F — MINI1CLK_REQ# / CARD_CLK_REQ# — MINI1CLK_REQ# 34 / CARD_CLK_REQ# 30
SRC-9 / SRC-9# — PCIE_MINI2 / PCIE_MINI2# — RP21 0 — CLK_PCIE_MINI2 33 / CLK_PCIE_MINI2# 33
SRC-10 / SRC-10# — PCIE_ICH / PCIE_ICH# — RP23 0 — CLK_PCIE_ICH 12 / CLK_PCIE_ICH# 12
CR#_H/SRC-11 / CR#_G/SRC-11# — PCIE_LOM / PCIE_LOM# — RP22 0 — CLK_PCIE_LOM 42 / CLK_PCIE_LOM# 42
GND 65

to ATI VGA

+3.3V_RUN
H_STP_PCI# R397 10K
H_STP_CPU# R396 10K

Silego need pull up
but other?

POP RESISTOR FOR UMA

DOT96_SSC / DOT96_SSC# — RP6 0_UMA — to MCH_DPLL_REF_CLK — MCH_DREFCLK 6 / MCH_DREFCLK# 6
27M_SS / 27M_NSS — RP14 0_UMA — to MCH_DPLL_REF_SSCLK — DREF_SSCLK 6 / DREF_SSCLK# 6
CPU_ITP / CPU_ITP# — RP15 0_NC — CLK_CPU_ITP 3 / CLK_CPU_ITP# 3
POP for ITP use

8

+3.3V_RUN
CLK_3GPLLREQ# R355 10K
SATA_CLKREQ# R356 10K
CARD_CLK_REQ# R398 10K
MINI1CLK_REQ# R399 10K
PCI_PCCARD R343 10K_NC

PCI_SIO R352 10K_NC
PCI_ICH R341 10K_NC

UMA without iAMT

+3.3V_RUN
L58 BLM21PG600SN1D 805 120 ohms@100Mhz
+CK_VDD_MAIN
C459 0.1U, C476 0.1U, C486 0.1U, C462 0.1U, C473 0.1U, C485 0.1U, C487 10U_NC
L51 BLM21PG600SN1D 805 120 ohms@100Mhz
R359 2.2 — +CK_VDD_PCI — C446 0.1U
R391 2.2 — +CK_VDD_PLL3 — C461 0.1U
R358 2.2 — +CK_VDD_48 — C448 0.1U, C447 4.7U
R377 2.2 — +CK_VDD_SRC 603 — C460 0.1U

Non-iAMT

SMbus address D2

These are for
backdrive issue.

+3.3V_RUN
RP3 2.2KX2
26,31,39 SMBDAT1 — Q40 2N7002W-7-F — CLK_SDATA
26,31,39 SMBCLK1 — Q39 2N7002W-7-F — CLK_SCLK

+3.3V_RUN
PCI_ICH — R339 10K_NC, R340 10K_NC

+3.3V_RUN
27M_SEL — R351 10K_DIS, R342 10K_UMA

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

27M_SEL

27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/ 100M_T	96/ 100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout

QUANTA COMPUTER

Title: CLOCK GENERATOR
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6 PCIE_MTX_GRX_P[0..15]
6 PCIE_MTX_GRX_N[0..15]

U43A

PART 1 OF 7

PCI-EXPRESS INTERFACE

PCIE_MTX_GRX_P0	AK33	PCIE_RX0P	PCIE_TX0P	AG31	PCIE_MRX_GTX_C_P0
PCIE_MTX_GRX_N0	AJ33	PCIE_RX0N	PCIE_TX0N	AG30	PCIE_MRX_GTX_C_N0
PCIE_MTX_GRX_P1	AJ35	PCIE_RX1P	PCIE_TX1P	AF31	PCIE_MRX_GTX_C_P1
PCIE_MTX_GRX_N1	AJ34	PCIE_RX1N	PCIE_TX1N	AF30	PCIE_MRX_GTX_C_N1
PCIE_MTX_GRX_P2	AH35	PCIE_RX2P	PCIE_TX2P	AF28	PCIE_MRX_GTX_C_P2
PCIE_MTX_GRX_N2	AH34	PCIE_RX2N	PCIE_TX2N	AF27	PCIE_MRX_GTX_C_N2
PCIE_MTX_GRX_P3	AG35	PCIE_RX3P	PCIE_TX3P	AD31	PCIE_MRX_GTX_C_P3
PCIE_MTX_GRX_N3	AG34	PCIE_RX3N	PCIE_TX3N	AD30	PCIE_MRX_GTX_C_N3
PCIE_MTX_GRX_P4	AF33	PCIE_RX4P	PCIE_TX4P	AD28	PCIE_MRX_GTX_C_P4
PCIE_MTX_GRX_N4	AF33	PCIE_RX4N	PCIE_TX4N	AD27	PCIE_MRX_GTX_C_N4
PCIE_MTX_GRX_P5	AE35	PCIE_RX5P	PCIE_TX5P	AB31	PCIE_MRX_GTX_C_P5
PCIE_MTX_GRX_N5	AE34	PCIE_RX5N	PCIE_TX5N	AB30	PCIE_MRX_GTX_C_N5
PCIE_MTX_GRX_P6	AD35	PCIE_RX6P	PCIE_TX6P	AB28	PCIE_MRX_GTX_C_P6
PCIE_MTX_GRX_N6	AD34	PCIE_RX6N	PCIE_TX6N	AB27	PCIE_MRX_GTX_C_N6
PCIE_MTX_GRX_P7	AC35	PCIE_RX7P	PCIE_TX7P	AA31	PCIE_MRX_GTX_C_P7
PCIE_MTX_GRX_N7	AC34	PCIE_RX7N	PCIE_TX7N	AA30	PCIE_MRX_GTX_C_N7
PCIE_MTX_GRX_P8	AB33	PCIE_RX8P	PCIE_TX8P	AA28	PCIE_MRX_GTX_C_P8
PCIE_MTX_GRX_N8	AA33	PCIE_RX8N	PCIE_TX8N	AA27	PCIE_MRX_GTX_C_N8
PCIE_MTX_GRX_P9	AA35	PCIE_RX9P	PCIE_TX9P	W31	PCIE_MRX_GTX_C_P9
PCIE_MTX_GRX_N9	AA34	PCIE_RX9N	PCIE_TX9N	W30	PCIE_MRX_GTX_C_N9
PCIE_MTX_GRX_P10	Y35	PCIE_RX10P	PCIE_TX10P	W28	PCIE_MRX_GTX_C_P10
PCIE_MTX_GRX_N10	Y34	PCIE_RX10N	PCIE_TX10N	W27	PCIE_MRX_GTX_C_N10
PCIE_MTX_GRX_P11	W35	PCIE_RX11P	PCIE_TX11P	V31	PCIE_MRX_GTX_C_P11
PCIE_MTX_GRX_N11	W34	PCIE_RX11N	PCIE_TX11N	V30	PCIE_MRX_GTX_C_N11
PCIE_MTX_GRX_P12	V33	PCIE_RX12P	PCIE_TX12P	V28	PCIE_MRX_GTX_C_P12
PCIE_MTX_GRX_N12	U33	PCIE_RX12N	PCIE_TX12N	V27	PCIE_MRX_GTX_C_N12
PCIE_MTX_GRX_P13	U35	PCIE_RX13P	PCIE_TX13P	U31	PCIE_MRX_GTX_C_P13
PCIE_MTX_GRX_N13	U34	PCIE_RX13N	PCIE_TX13N	U30	PCIE_MRX_GTX_C_N13
PCIE_MTX_GRX_P14	T35	PCIE_RX14P	PCIE_TX14P	U28	PCIE_MRX_GTX_C_P14
PCIE_MTX_GRX_N14	T34	PCIE_RX14N	PCIE_TX14N	U27	PCIE_MRX_GTX_C_N14
PCIE_MTX_GRX_P15	R35	PCIE_RX15P	PCIE_TX15P	R31	PCIE_MRX_GTX_C_P15
PCIE_MTX_GRX_N15	R34	PCIE_RX15N	PCIE_TX15N	R30	PCIE_MRX_GTX_C_N15

Clock

17 CLK_PCIE_VGA — AJ31 PCIE_REFCLKP
17 CLK_PCIE_VGA# — AJ30 PCIE_REFCLKN

SM Bus

AK35 NC_SMB_DATA
AK34 NC_SMBCLK

13 PLTRST_DELAY# — R718 402 0_DIS — AM32 PERSTB

Calibration

PCIE_CALRN — AG26 — R131 402 2K/F_DIS — +PCIE_VDDC
PCIE_CALRP — AJ27

NC_DRAM_0 — AF3
NC_DRAM_1 — AG9
NC_AC_BATT — AK29
NC_FAN_TACH — AK14

R126 1.27K_DIS 402

M86-LP_DIS

6 PCIE_MRX_GTX_P[0..15]
6 PCIE_MRX_GTX_N[0..15]

PCIE_MRX_GTX_P0	C213	0.1U_0805	PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_P1	C231	0.1U_0805	PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_P2	C233	0.1U_0805	PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_P3	C211	0.1U_0805	PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_P4	C230	0.1U_0805	PCIE_MRX_GTX_C_P4
PCIE_MRX_GTX_P5	C210	0.1U_0805	PCIE_MRX_GTX_C_P5
PCIE_MRX_GTX_P6	C208	0.1U_0805	PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_P7	C227	0.1U_0805	PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_P8	C206	0.1U_0805	PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_P9	C226	0.1U_0805	PCIE_MRX_GTX_C_P9
PCIE_MRX_GTX_P10	C224	0.1U_0805	PCIE_MRX_GTX_C_P10
PCIE_MRX_GTX_P11	C204	0.1U_0805	PCIE_MRX_GTX_C_P11
PCIE_MRX_GTX_P12	C220	0.1U_0805	PCIE_MRX_GTX_C_P12
PCIE_MRX_GTX_P13	C222	0.1U_0805	PCIE_MRX_GTX_C_P13
PCIE_MRX_GTX_P14	C200	0.1U_0805	PCIE_MRX_GTX_C_P14
PCIE_MRX_GTX_P15	C201	0.1U_0805	PCIE_MRX_GTX_C_P15
PCIE_MRX_GTX_N0	C214	0.1U_0805	PCIE_MRX_GTX_C_N0
PCIE_MRX_GTX_N1	C232	0.1U_0805	PCIE_MRX_GTX_C_N1
PCIE_MRX_GTX_N2	C234	0.1U_0805	PCIE_MRX_GTX_C_N2
PCIE_MRX_GTX_N3	C212	0.1U_0805	PCIE_MRX_GTX_C_N3
PCIE_MRX_GTX_N4	C229	0.1U_0805	PCIE_MRX_GTX_C_N4
PCIE_MRX_GTX_N5	C209	0.1U_0805	PCIE_MRX_GTX_C_N5
PCIE_MRX_GTX_N6	C207	0.1U_0805	PCIE_MRX_GTX_C_N6
PCIE_MRX_GTX_N7	C228	0.1U_0805	PCIE_MRX_GTX_C_N7
PCIE_MRX_GTX_N8	C205	0.1U_0805	PCIE_MRX_GTX_C_N8
PCIE_MRX_GTX_N9	C225	0.1U_0805	PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_N10	C223	0.1U_0805	PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_N11	C203	0.1U_0805	PCIE_MRX_GTX_C_N11
PCIE_MRX_GTX_N12	C219	0.1U_0805	PCIE_MRX_GTX_C_N12
PCIE_MRX_GTX_N13	C221	0.1U_0805	PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_N14	C199	0.1U_0805	PCIE_MRX_GTX_C_N14
PCIE_MRX_GTX_N15	C202	0.1U_0805	PCIE_MRX_GTX_C_N15

QUANTA COMPUTER

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MEMORY APERTURE SIZE SELECT

MEMORY SIZE	CFG3 GPIO9	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	X	0	0	0
256MB	X	0	0	1
64MB	X	0	1	0
512MB	X	1	0	0

Memory Straps	RAM_ TYPE_CFG3	RAM_ TYPE_CFG2	RAM_ TYPE_CFG1	RAM_ TYPE_CFG0
400 MHz 256MB(16M*16) Hynix	1	1	1	1
400 MHz 256MB(16M*16) Qimonda	1	1	1	0
500 MHz 256MB(16M*16) Hynix	1	1	0	1
500 MHz 256MB(16M*16) Qimonda	1	1	0	0
500 MHz 256MB(16M*16) Samsung	1	0	1	1

8/15: The strap on VIP[3] is for enabling HD Audio on M86.

U43B — PART 2 OF 7 — M86-LP-DIS

HDMI CONN

VRAM SIZE

VRAM TYPE

LVDS

HDMI

CRT

DIS only

Layout Note: Place 150 ohm termination resistors close to ATI CHIP.

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QUANTA COMPUTER

Title: VGA-G86GLM (VIDEO)

Size: | Document Number: GM3 | Rev: 2B

Date: Friday, January 18, 2008 | Sheet 19 of 62

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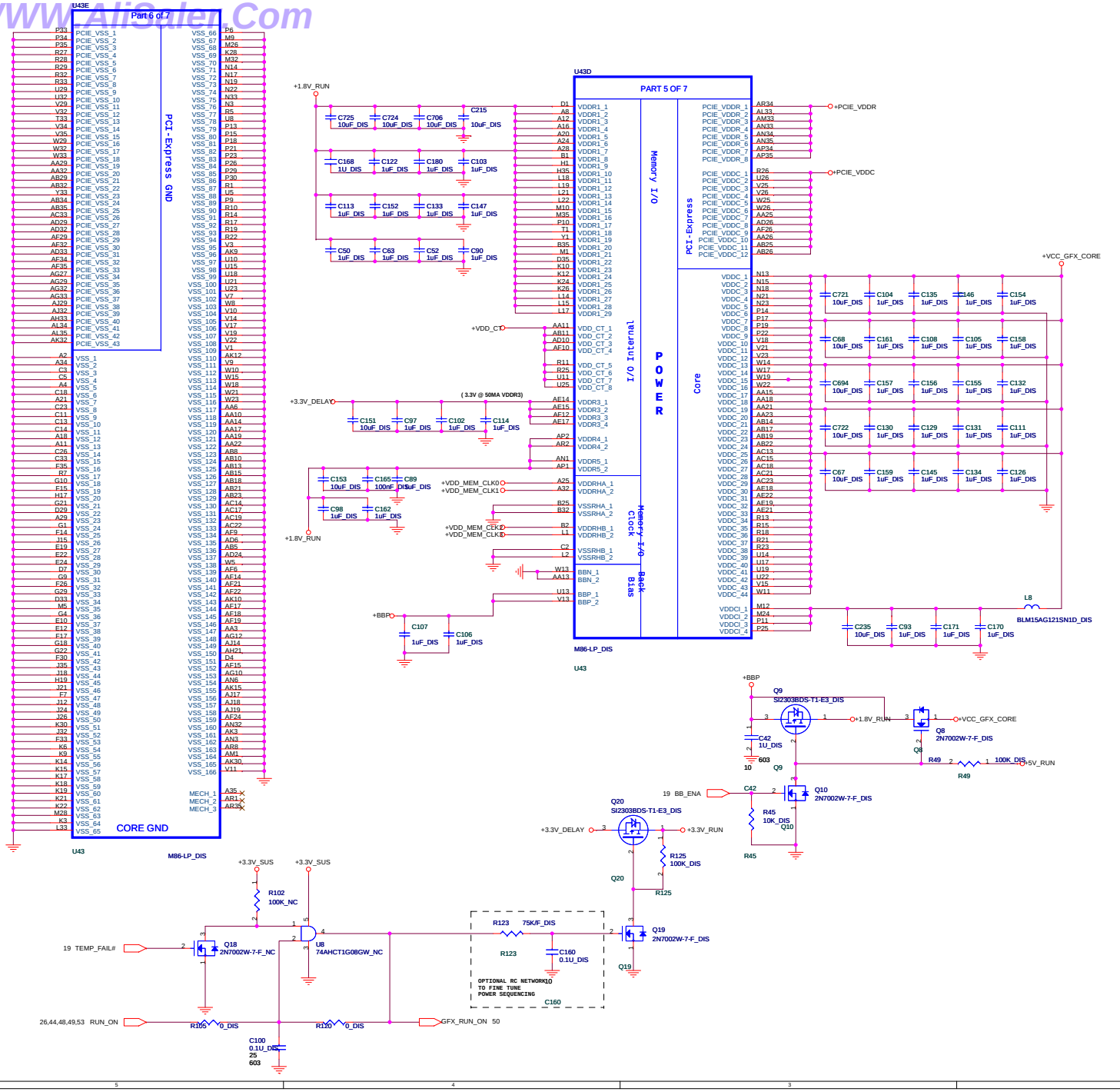

QUANTA COMPUTER

Title	VGA-G86GLM (VIDEO)		
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LVDS

+LVDDR — R129 0_DIS

+1.8V_RUN — BLM18PG471SN1D_DIS L12 — C183 10uF_DIS, C185 100nF_DIS, C186 100nF_DIS — +LVDDC (1.8V @ 400MA LVDDC,LVDDR)

+1.8V_RUN — L11 BLM15BD121SN1D_DIS L11 — C166 10uF_DIS, C164 1uF_DIS, C163 100nF_DIS — +LPVDD (1.8V @ 30MA LPVDD)

PLL_CLK

+1.8V_RUN — BLM15BD121SN1D_DIS L69 — C752 10uF_DIS, C753 1uF_DIS, C754 100nF_DIS — +DPLL_PVDD (1.8V @ 40MA DPLL_PVDD)

+1.8V_RUN — BLM15BD121SN1D_DIS L21 — C244 10uF_DIS, C248 1uF_DIS, C257 100nF_DIS — +PCIE_PVDD (1.8V @ 40MA PCIE_PVDD)

+1.8V_RUN — BLM15BD121SN1D_DIS L71 — C765 10uF_DIS, C764 1uF_DIS, C763 100nF_DIS — +A2VDDQ (1.8V @ 2MA A2VDDQ)

DAC(CRT)

+1.8V_RUN — BLM15BD121SN1D_DIS L74 — C775 10uF_DIS, C776 100nF_DIS, C184 1uF_DIS — +VDD1DI, +VDD2DI (1.8V @ 100MA VDD1DI)

+1.8V_RUN — BLM15BD121SN1D_DIS L14 — C187 10uF_DIS, C193 100nF_DIS, C192 1uF_DIS — +AVDD (1.8V @ 65MA AVDD)

+1.8V_RUN — BLM15BD121SN1D_DIS L65 — C741 10uF_DIS, C739 100nF_DIS, C738 1uF_DIS — +TPVDD (1.8V @ 20 MA SINGLE LINK 1X4DP and 40mA for Dual-Link 2X4DP)

+1.8V_RUN — BLM15BD121SN1D_DIS L22 — C260 10uF_DIS, C95 100nF_DIS, C173 1uF_DIS — +VDD_CT (VDD_CT 1.8V @ 110MA (VDD_CT)

+1.8V_RUN — BLM18PG471SN1D_DIS L75 — C810 10uF_DIS, C800 1uF_DIS, C798 100nF_DIS — +PCIE_VDDR (1.8V @ 400MA PCIE_VDDR)

MEM IO CLK

+1.8V_RUN — BLM15BD121SN1D_DIS L79 — C181 10uF_DIS, C179 1uF_DIS, C182 100nF_DIS — +VDD_MEM_CLK0 (1.8V @ MA VDDRHA_1 INCLUDED IN VDDR1)

+1.8V_RUN — BLM15BD121SN1D_DIS L78 — C811 10uF_DIS, C808 1uF_DIS, C809 100nF_DIS — +VDD_MEM_CLK1 (1.8V @ MA VDDRHA_2 INCLUDED IN VDDR1)

+1.8V_RUN — BLM15BD121SN1D_DIS L63 — C717 10uF_DIS, C718 1uF_DIS, C719 100nF_DIS — +VDD_MEM_CLK2 (1.8V @ MA VDDRHB_1 INCLUDED IN VDDR1)

+1.8V_RUN — BLM15BD121SN1D_DIS L6 — C65 10uF_DIS, C72 1uF_DIS, C66 100nF_DIS — +VDD_MEM_CLK3 (1.8V @ MA VDDRHB_2 INCLUDED IN VDDR1)

TMDS

+1.1V_GFX_PCIE — BLM15BD121SN1D_DIS L68 — C743 10uF_DIS, C745 100nF_DIS, C744 1uF_DIS — +DPA_VDDR (1.1V @ 200MA EACH SINGLE LINK)

+1.1V_GFX_PCIE — BLM15BD121SN1D_DIS L10 — C150 10uF_DIS, C149 100nF_DIS, C148 1uF_DIS — +DPB_VDDR (1.1V @ 200MA EACH SINGLE LINK)

+1.1V_GFX_PCIE — BLM18PG121SN1D_DIS L18 — C245 10uF_DIS, C174 1uF_DIS, C177 100nF_DIS; C176 1uF_DIS, C175 1uF_DIS, C178 1uF_DIS — +PCIE_VDDC (PCIE_VDDC 1.1V @ 1A)

BLM15BD121SN1D_DIS L9 — C125 10uF_DIS, C123 1uF_DIS, C124 100nF_DIS — +DPLL_VDDC (DPLL_VDDC 1.1V @ 100 MA)

+VCC_GFX_CORE — BLM18PG471SN1D_DIS L67 — C101 10uF_DIS, C110 1uF_DIS, C109 100nF_DIS — +MPVDD (.95V-1.1V @ 345MA MPVDD)

+3.3V_DELAY — BLM15BD121SN1D_DIS L73 — C771 10uF_DIS, C769 100nF_DIS, C770 1uF_DIS — +A2VDD (3.3V @ 135MA A2VDD)

PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE

QUANTA COMPUTER

Title	VGA-G86GLM (VIDEO)	
Size	Document Number GM3	Rev 2B
Date: Friday, January 18, 2008	Sheet 21 of 62	

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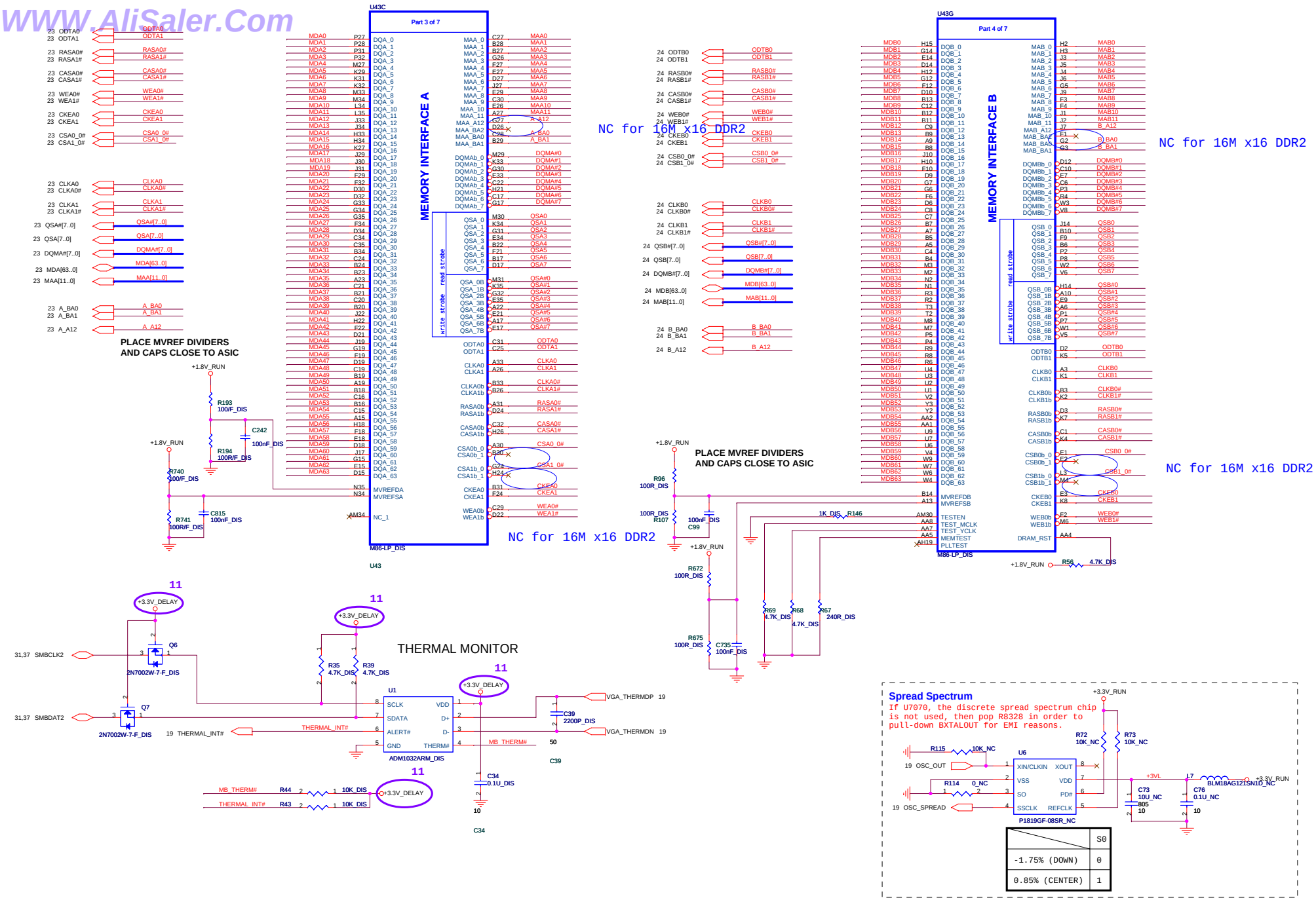

QUANTA COMPUTER

Title	VGA-M82-S (PCIe)
Size	Document Number GM3
Rev	2B
Date: Friday, January 18, 2008	Sheet 22 of 62

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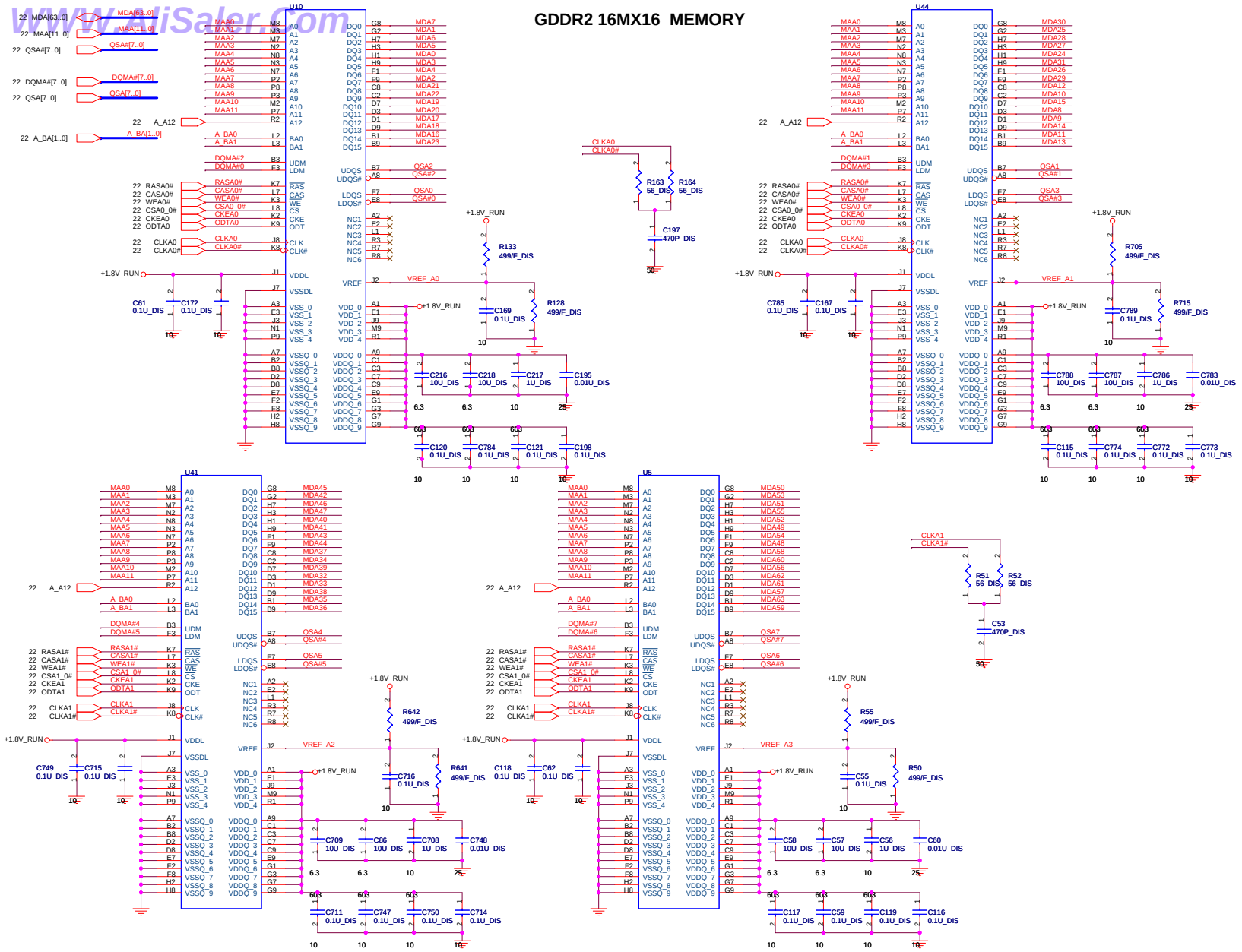
GDDR2 16MX16 MEMORY



QUANTA COMPUTER

Title	VGA-M82-S (VRAM)	
Size	Document Number GM3	Rev 2B
Date: Friday, January 18, 2008	Sheet 23 of 62	

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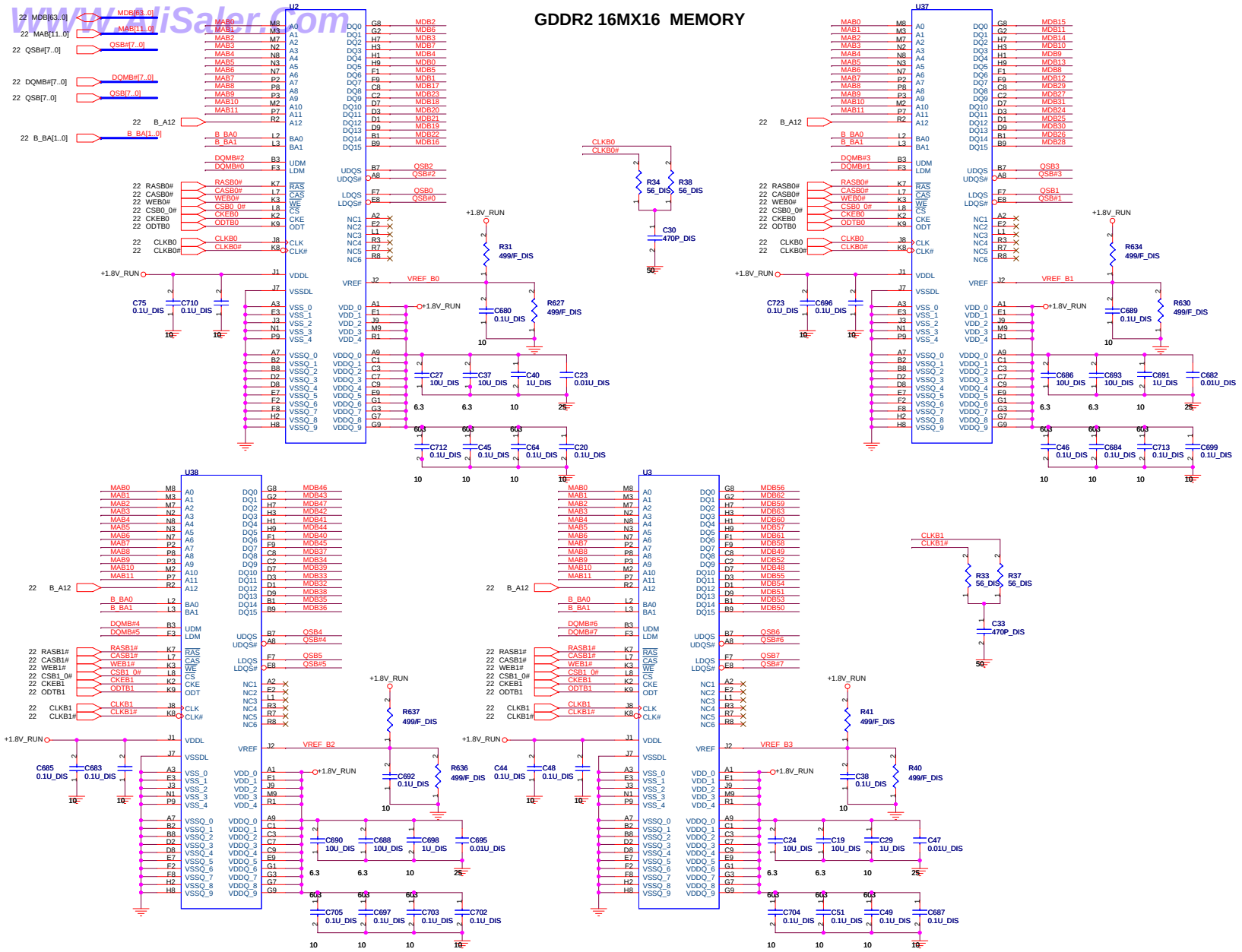
GDDR2 16MX16 MEMORY



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QUANTA COMPUTER

Title	VGA-M82-S (VRAM)		
Size	Document Number GM3		Rev 2B
Date: Friday, January 18, 2008		Sheet 24 of 62	

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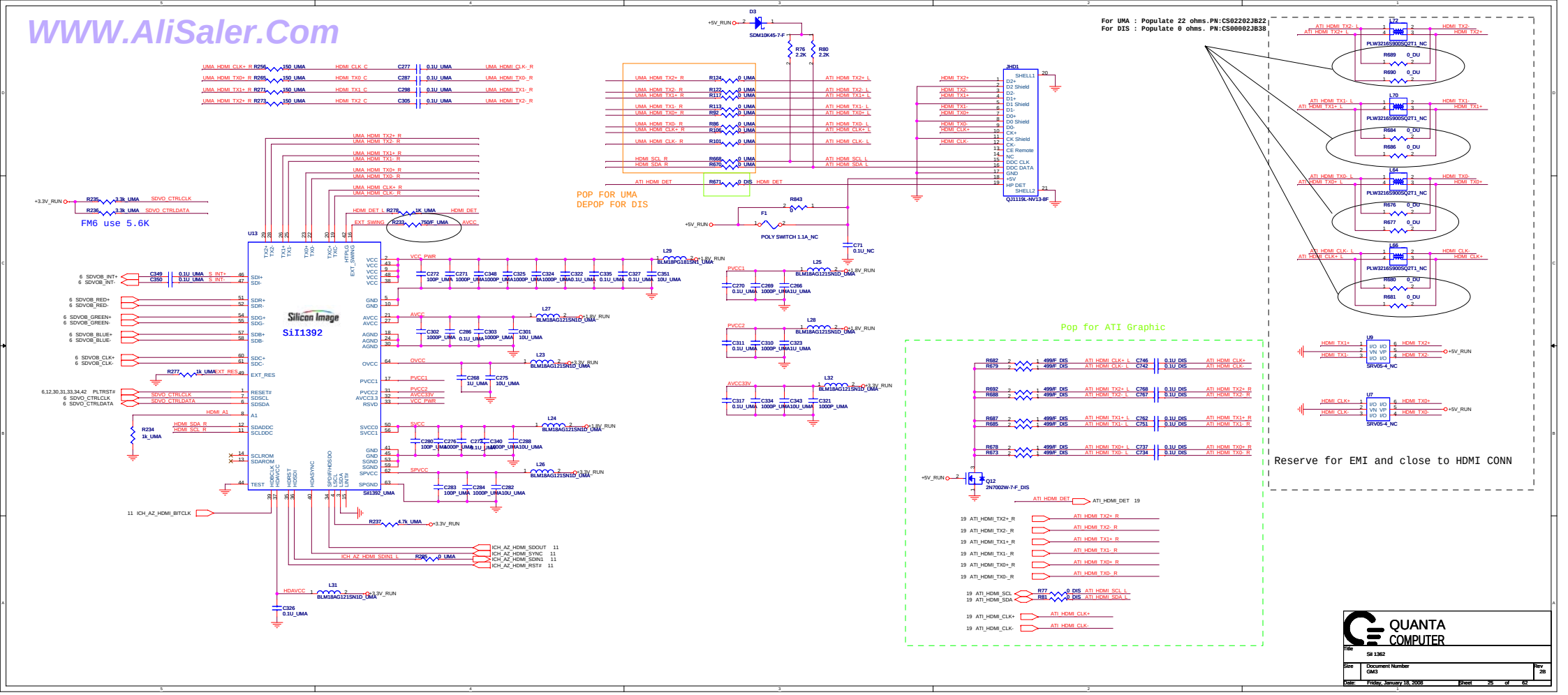
For UMA : Populate 22 ohms.PN:CS02202JB22
For DIS : Populate 0 ohms. PN:CS00002JB38



QUANTA COMPUTER

Title	Sil 1362		
Size	Document Number CM3		Rev 2B
Date: Friday, January 18, 2008	Sheet 25 of 62		

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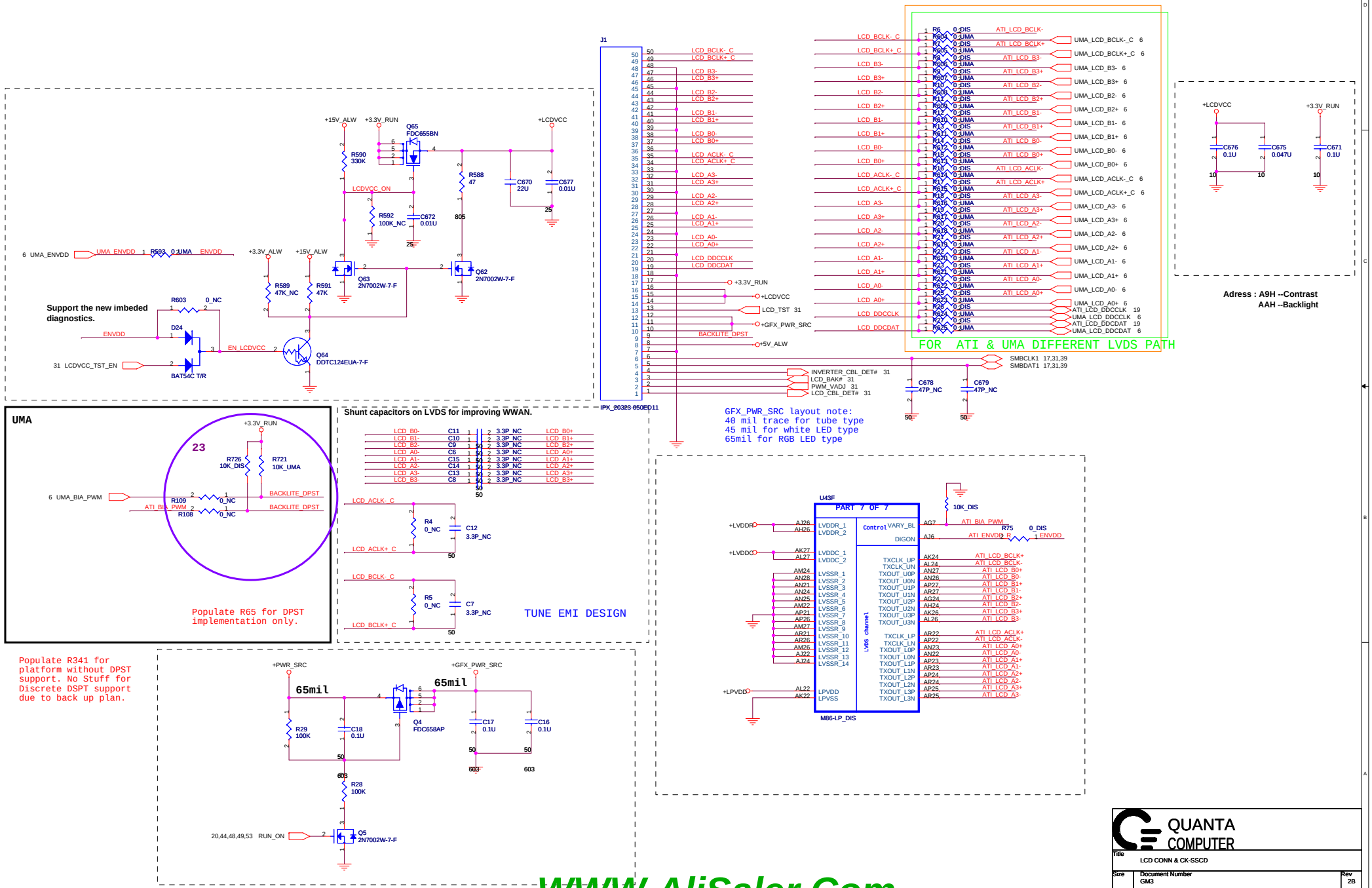

QUANTA COMPUTER

Title	LCD CONN & CK-SSCD
Size	Document Number GM3
Rev	2B
Date:	Friday, January 18, 2008
Sheet	26 of 62

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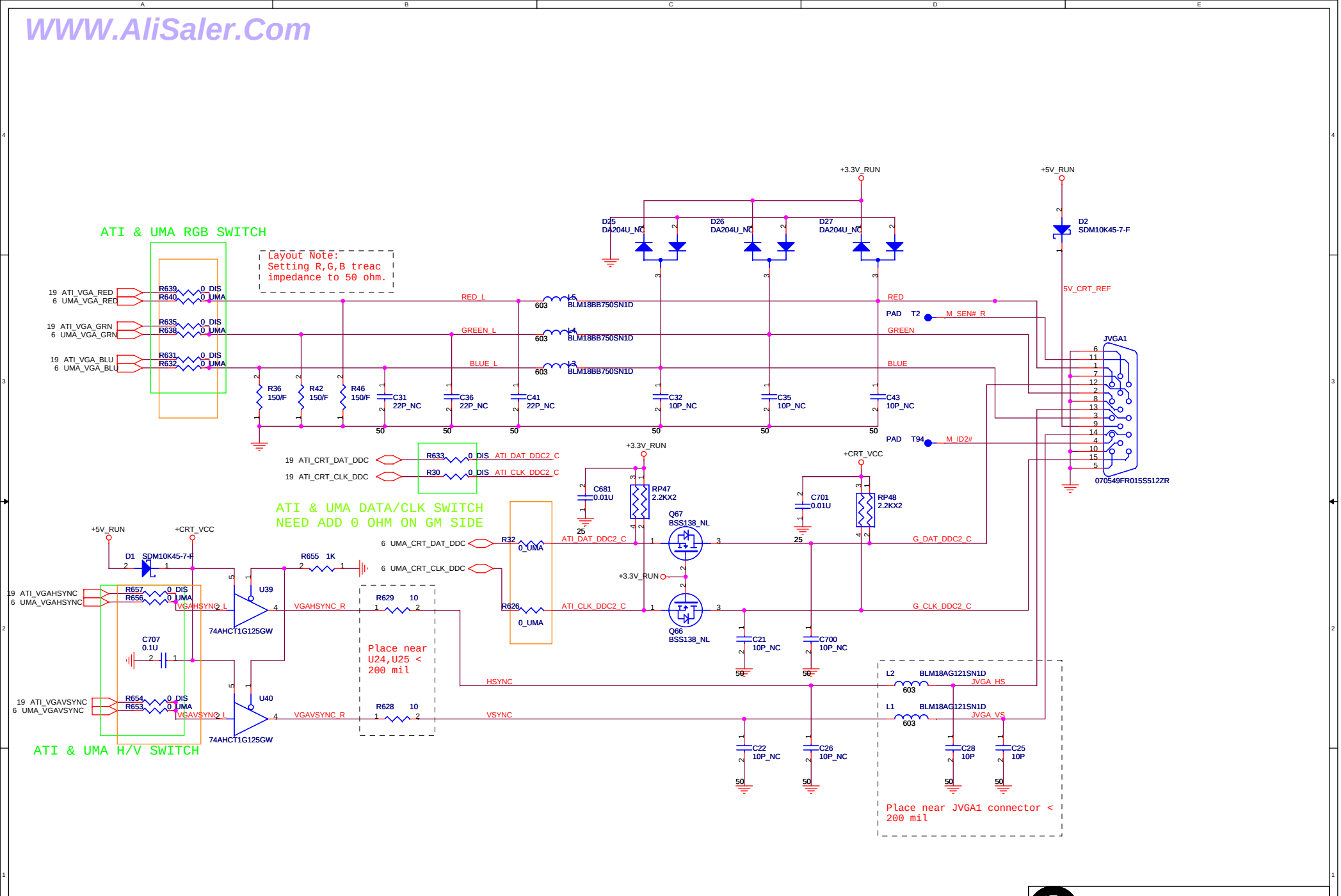

QUANTA COMPUTER

Title	CRT&TV CONN	
Size	Document Number GM3	Rev 2B
Date: Friday, January 18, 2008	Sheet 27 of 62	

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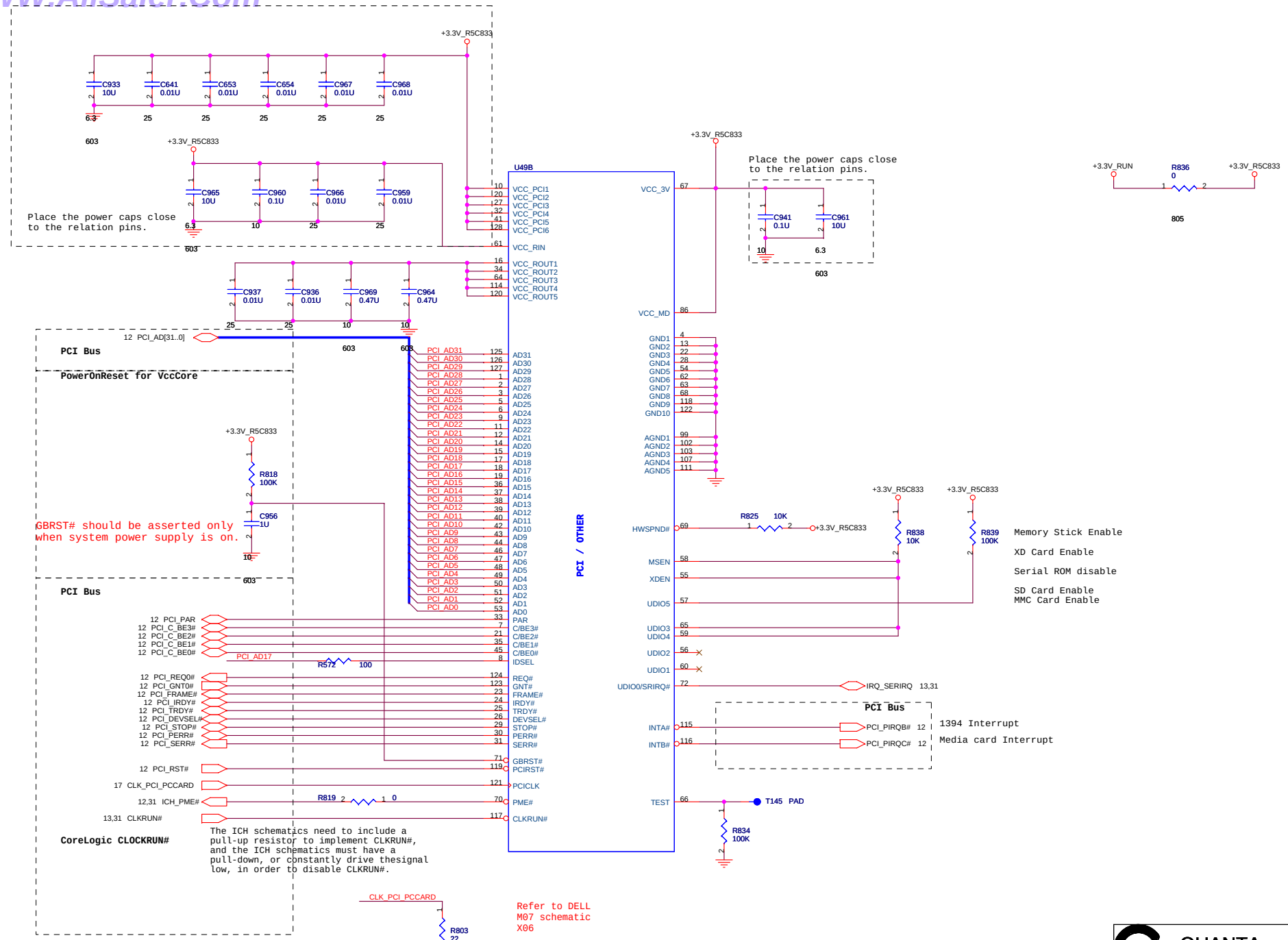

QUANTA COMPUTER

Title	8 IN 1 CONTROLLER
Size	Document Number GM3
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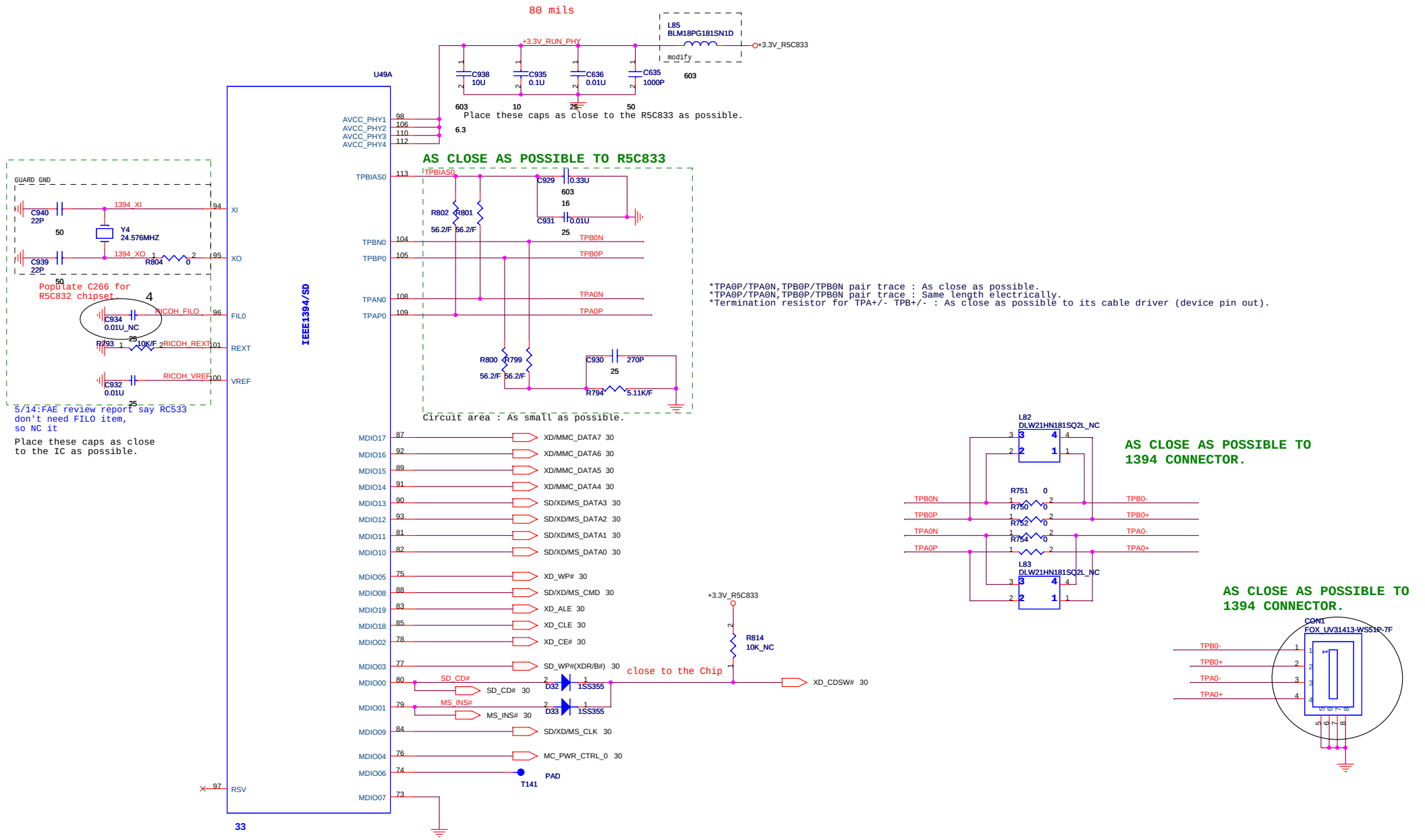

QUANTA COMPUTER

Title	IEEE 1394	
Size	Document Number GM3	Rev 2B
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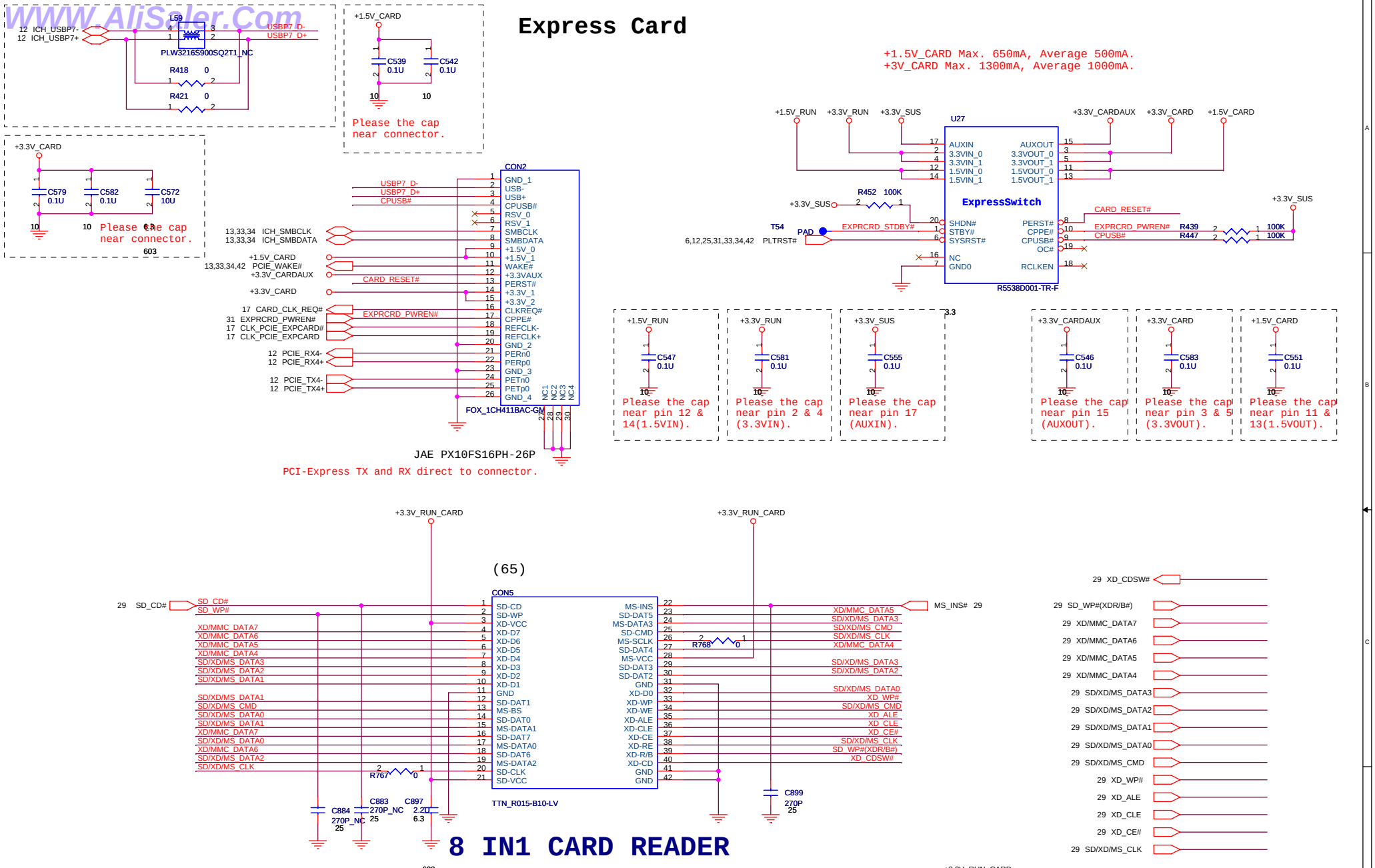
Express Card

+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



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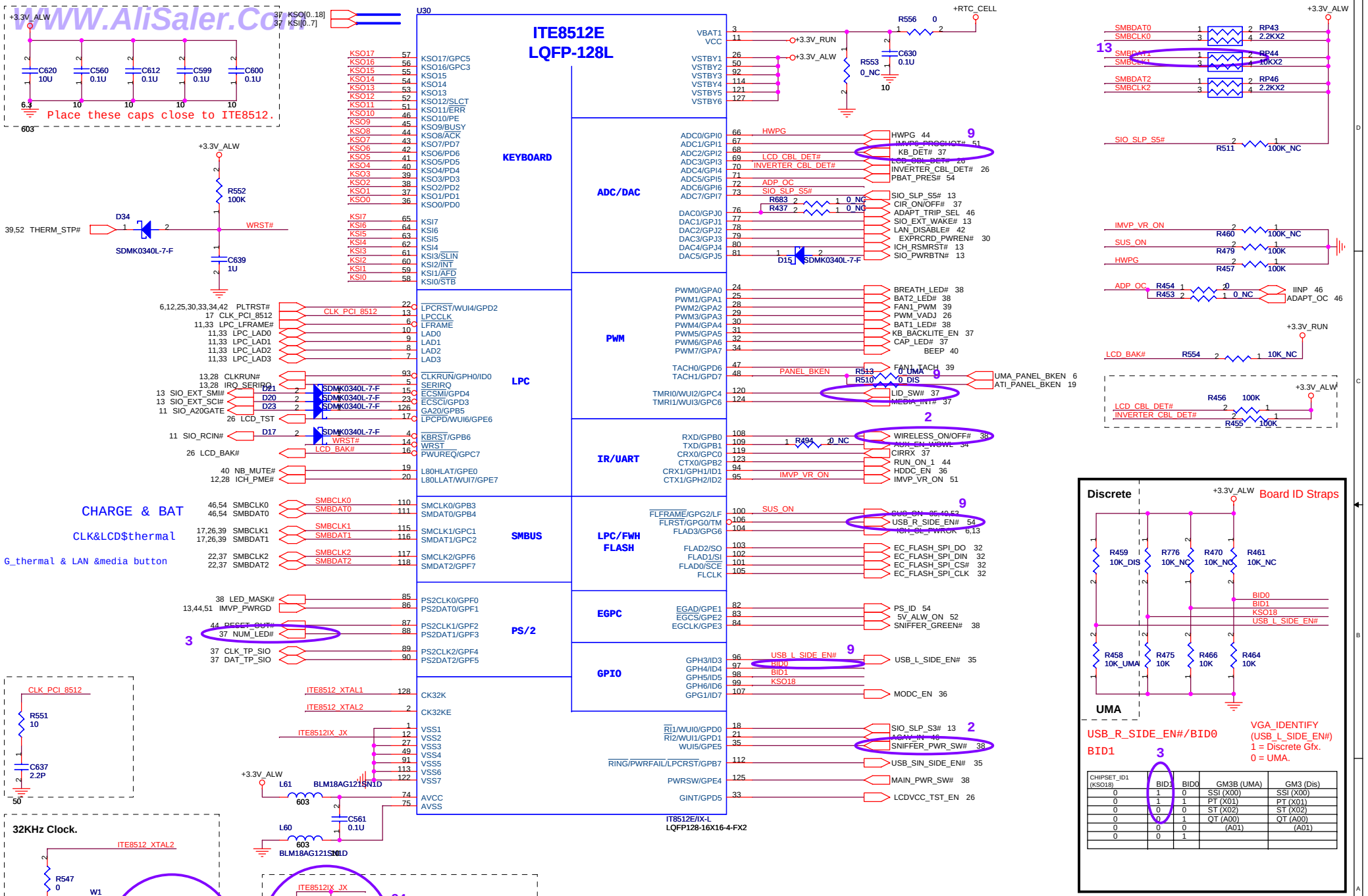
WWW.AliSaler.Com



CHIPSET_ID1 (KSO18)	BID1	BID0	GM3B (UMA)	GM3 (Dis)
0	1	0	SSI (X00)	SSI (X00)
0	1	1	PT (X01)	PT (X01)
0	0	0	ST (X02)	ST (X02)
0	0	1	QT (A00)	QT (A00)
0	0	0	(A01)	(A01)
0	0	1		

QUANTA COMPUTER

Title: Ultra I/O Controller ITE 8512

Size: | Document Number: GM3 | Rev: 2B

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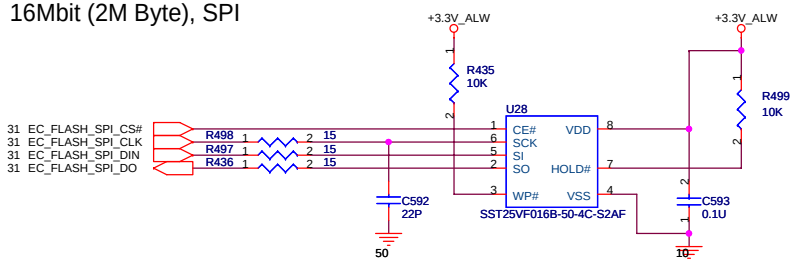
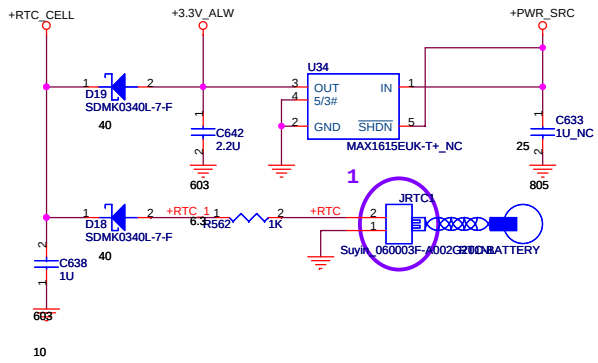
16Mbit (2M Byte), SPI



RTC BATTERY



QUANTA COMPUTER

Title	Ultra I/O Controller ECE5028	
Size	Document Number GM3	Rev 2B
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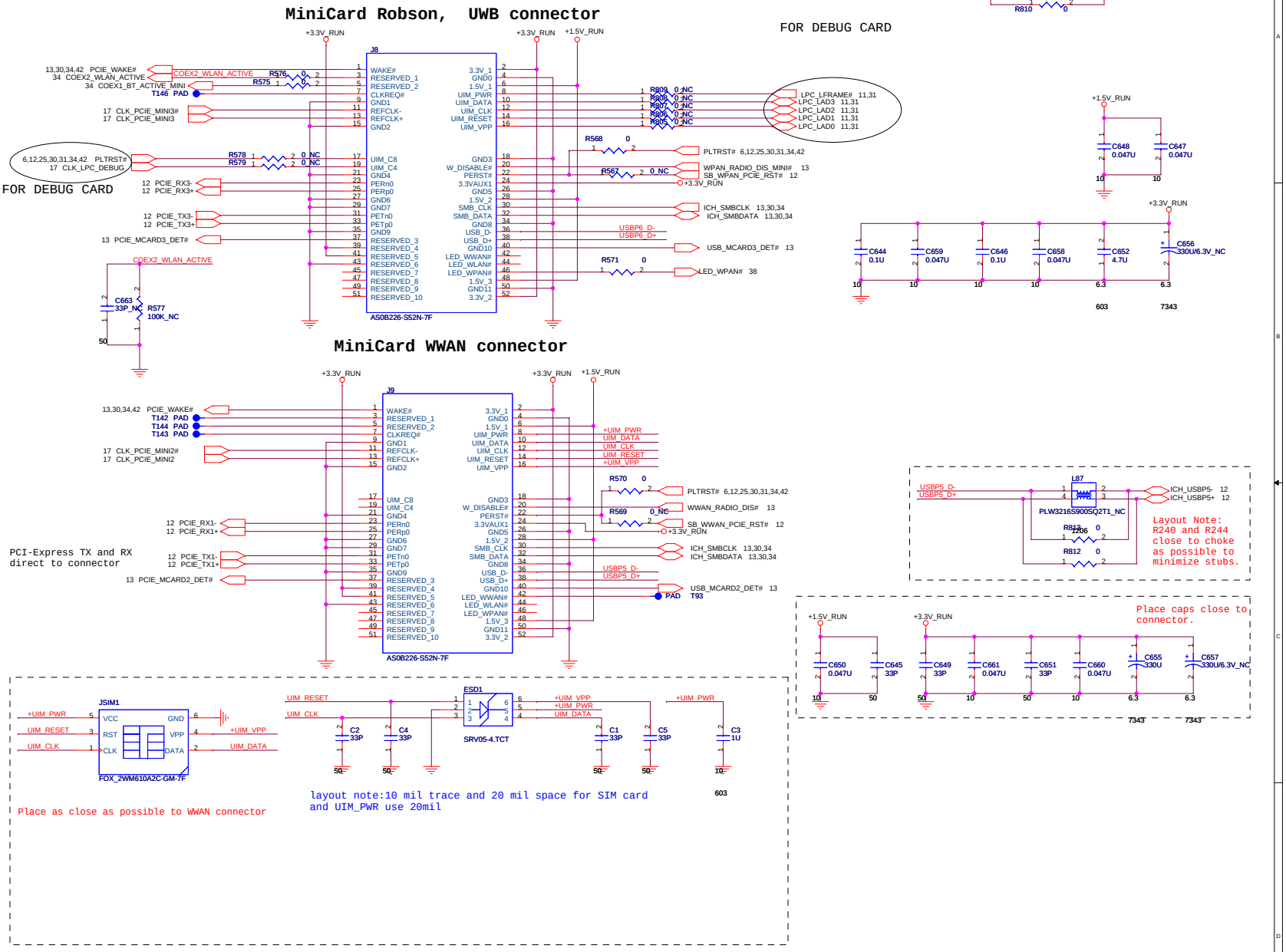

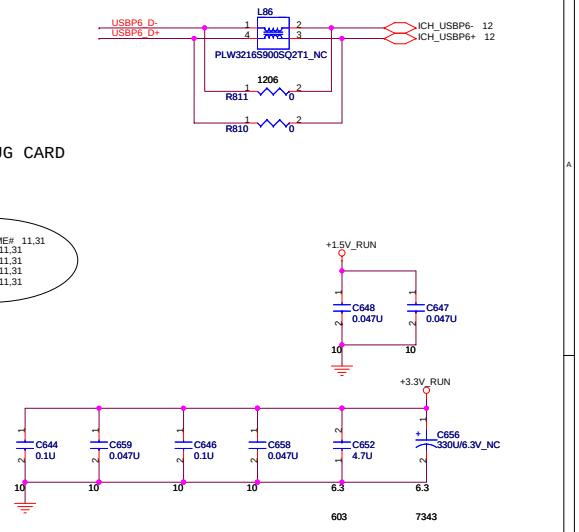

QUANTA COMPUTER

Title	WWAN, WPAN	
Size	Document Number GM3	Rev 2B
Date: Saturday, January 19, 2008	Sheet 33 of 62	

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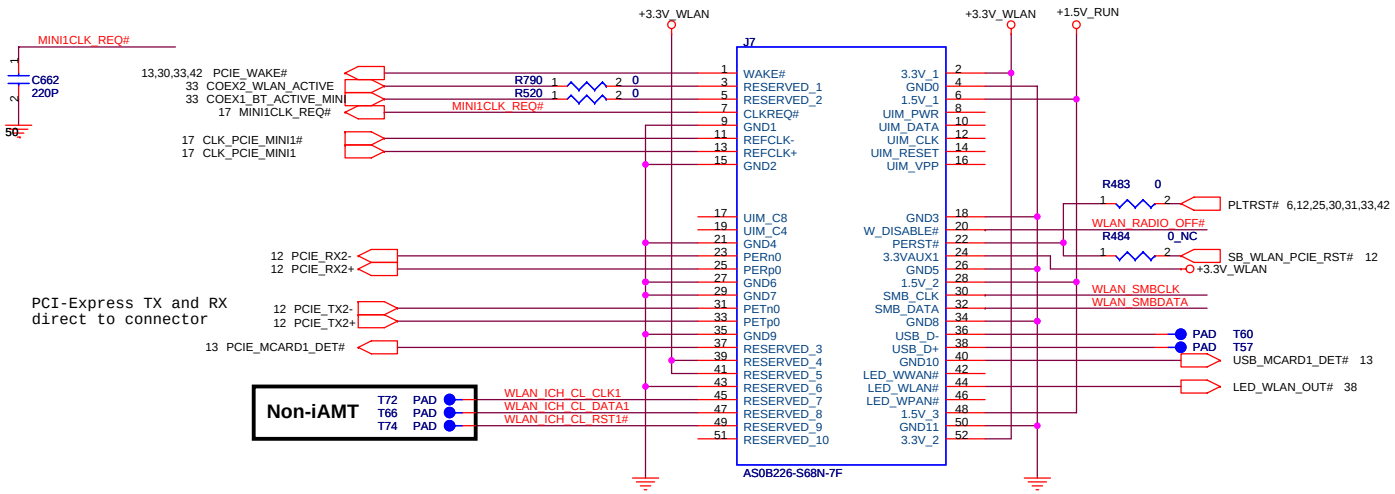
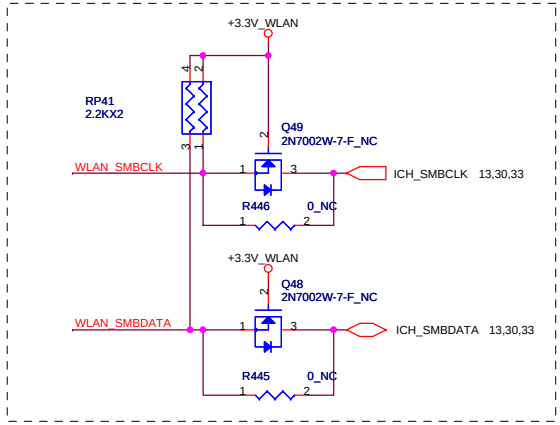
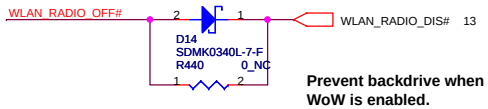
MiniCard WLAN connector

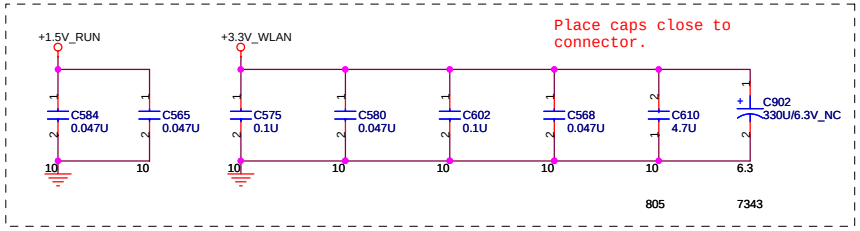


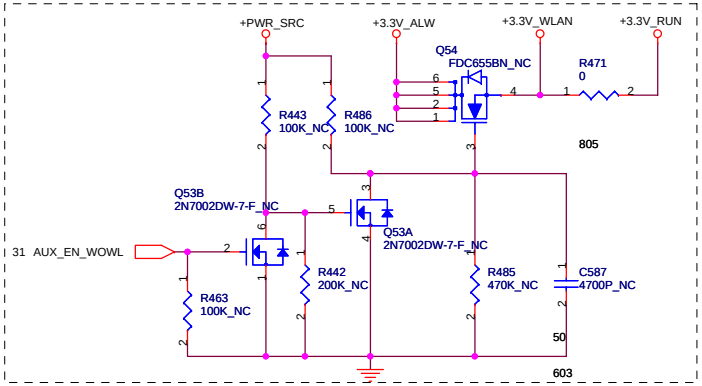


Suport for WoW



Prevent backdrive when WoW is enabled.





QUANTA COMPUTER

Title	WLAN	
Size	Document Number GM3	Rev 2B
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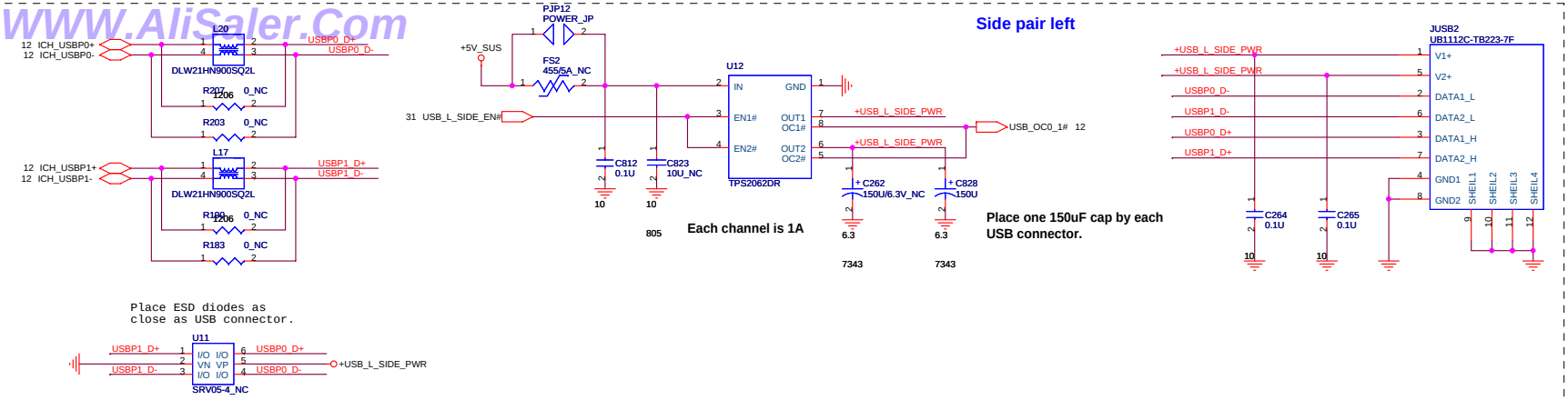
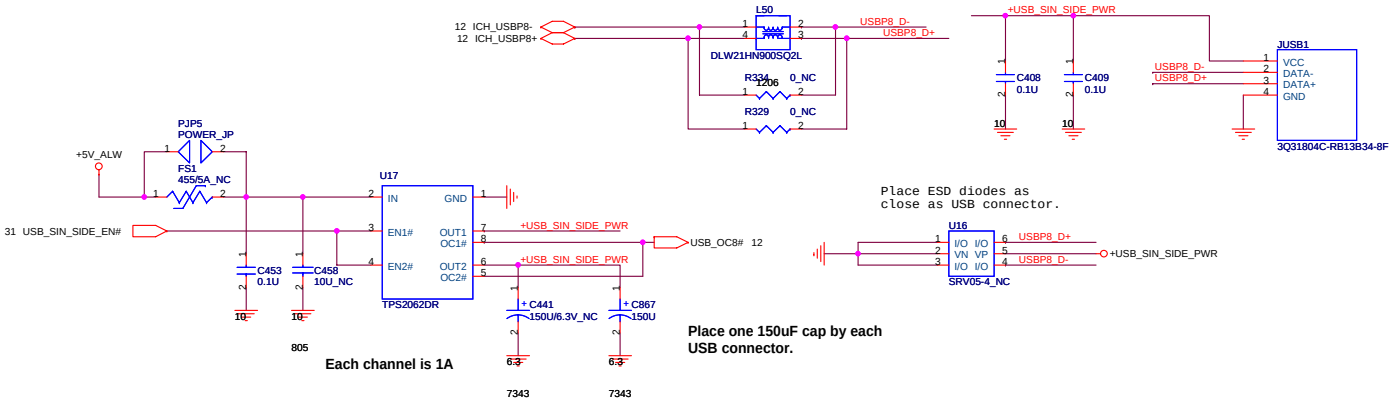
Side pair left



left side single USB port

22



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QUANTA COMPUTER

Title	External USB	
Size	Document Number GM3	Rev 2B
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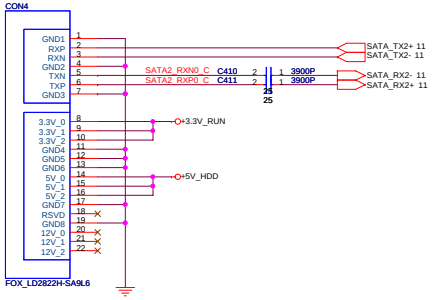
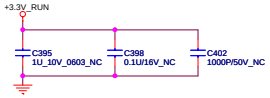
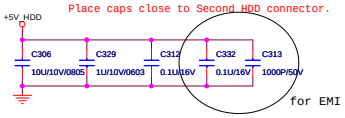
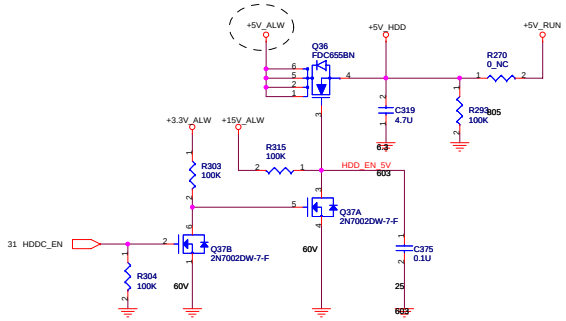
Second HDD

SATA Connector.

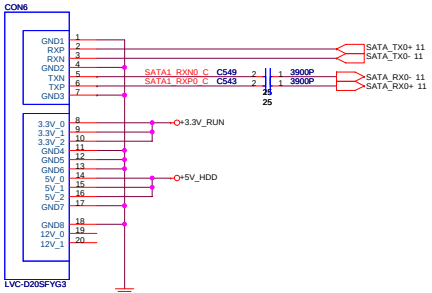


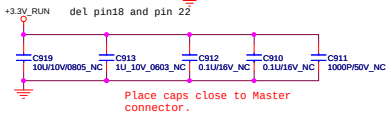


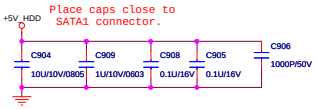




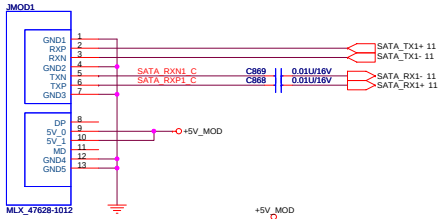
Master

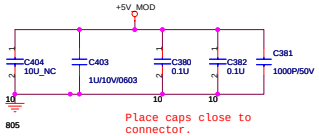


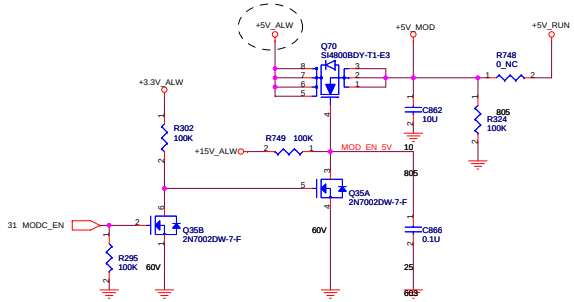




ODD Connector







QUANTA COMPUTER

Title	SATA (HDD&CD_ROM)	
Size	Document Number GM3	Rev 2B
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Touch Pad

17

+3.3V_ALW, +3.3V_ALW, +5V_RUN

RP19 4.7KX2

R393 100K

31 LID_SW#

JTP1

31 CLK_TP_SIO
31 DAT_TP_SIO

L56 603 BLM11A601S
L57 BLM11A601S
603

TP_CLK
TP_DATA

+5V_RUN

C478 10P, C479 10P, C475 10P, C474 10P, C436 0.1U, C434 0.047U, C437 0.1U, C920 0.047U

ACES_88502-0601

KEYBOARD CONNECTOR

31 KSO[0..18]
31 KSI[0..7]

31 KB_DET#

+3.3V_ALW

R276 100K

JKB1

KSI7, KSI6, KSI4, KSI2, KSI5, KSI1, KSI3, KSI0, KSO5, KSO4, KSO7, KSO6, KSO8, KSO3, KSO1, KSO2, KSO0, KSO12, KSO16, KSO15, KSO13, KSO14, KSO9, KSO11, KSO10, KSO17, KSO18

CAP_LED_R R275 220
NUM_LED_R R274 220

HRS_FH28D-64(32)SB-1SH(86)

Media Button

8/17:add dioad to protect GPIO port

10

+3.3V_ALW

DA204U_NC D11

+3.3V_ALW, +5V_ALW

+3.3V_ALW

R259 100K_0402

31 MEDIA_INT#

R266 10K_0402

C278 1U/10V/0603

22,31 SMBCLK2
22,31 SMBDAT2

38 HDD_LED
38 WLAN_LED
38 BT_LED

JMB1

5V_PWR, CLK, DAT, INT, GND, LED1, LED2, LED3, 3V_PWR, 5V_LED

ACES_88501-1001

C285 10U 4 805

29

FOR EMI

CP1: KSO10, KSO17, KSO18 — 100PX4_NC

CP3: KSO0, KSO12, KSO16, KSO15 — 100PX4_NC

CP2: KSO13, KSO14, KSO9, KSO11 — 100PX4_NC

CP5: KSO5, KSO4, KSO7, KSO6 — 100PX4_NC

CP4: KSO8, KSO3, KSO1, KSO2 — 100PX4_NC

CP7: KSI7, KSI6, KSI4, KSI2 — 100PX4_NC

CP6: KSI5, KSI1, KSI3, KSI0 — 100PX4_NC

100P CAPS CLOSE TO JKB1

Consumer IR

+3.3V_ALW, +3.3V_ALW

R585 100, R840 10K

31 CIRRX

CIRRX
CIR_VCC

U36

IRTX, VCC, GND1, GND2

SIL_TSOP36136TS

C667 4.7U, C666 0.1U

805

+5V_ALW, +3.3V_ALW

R844 10K_NC

Q32 2N7002W-7-F_NC

31 CIR_ON/OFF#

Q78 DDTC124EUA-7-F_NC

CIR_VCC

14

+3.3V_RUN, +5V_RUN

R254 100K

31 CAP_LED#

Q31 2N7002W-7-F

Q34 DDTA114YUA-7-F

CAP_LED_R

+3.3V_RUN, +5V_RUN

R263 100K

31 NUM_LED#

Q30 2N7002W-7-F

Q33 DDTA114YUA-7-F

NUM_LED_R

Key board Illumination

+5V_RUN, +KB_LED

FS3 1206L050YR

R252 33_NC

+KB_LED

J4

LED_PWM

88502-0401

+KB_LED

C921 0.1U

Q46 SI2304BDS-T1-E3

LED_PWM

31 KB_BACKLITE_EN

QUANTA COMPUTER

Title: TOUCH PAD, BULE TOOTH & FIR

Size | Document Number GM3 | Rev 2B

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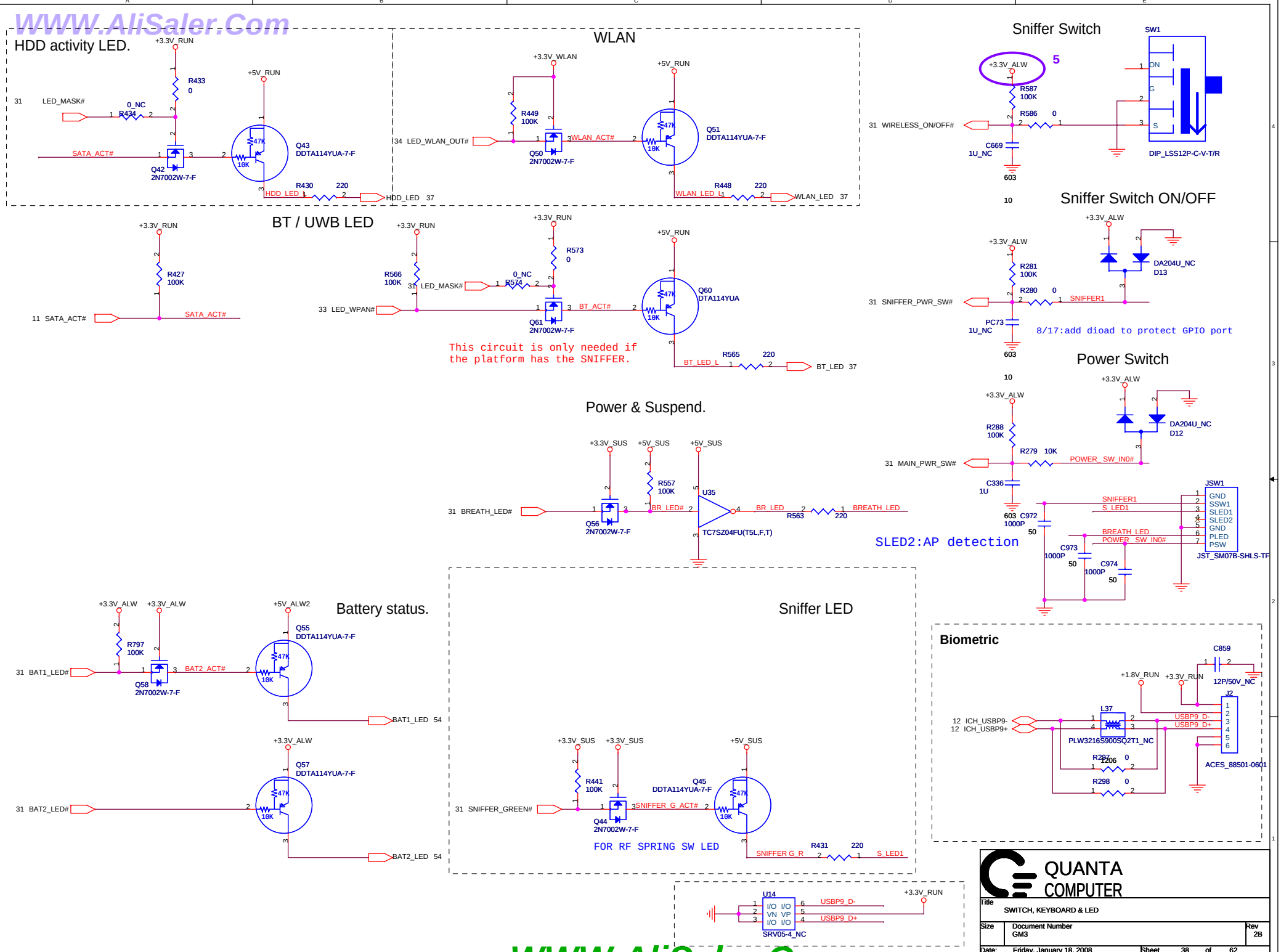

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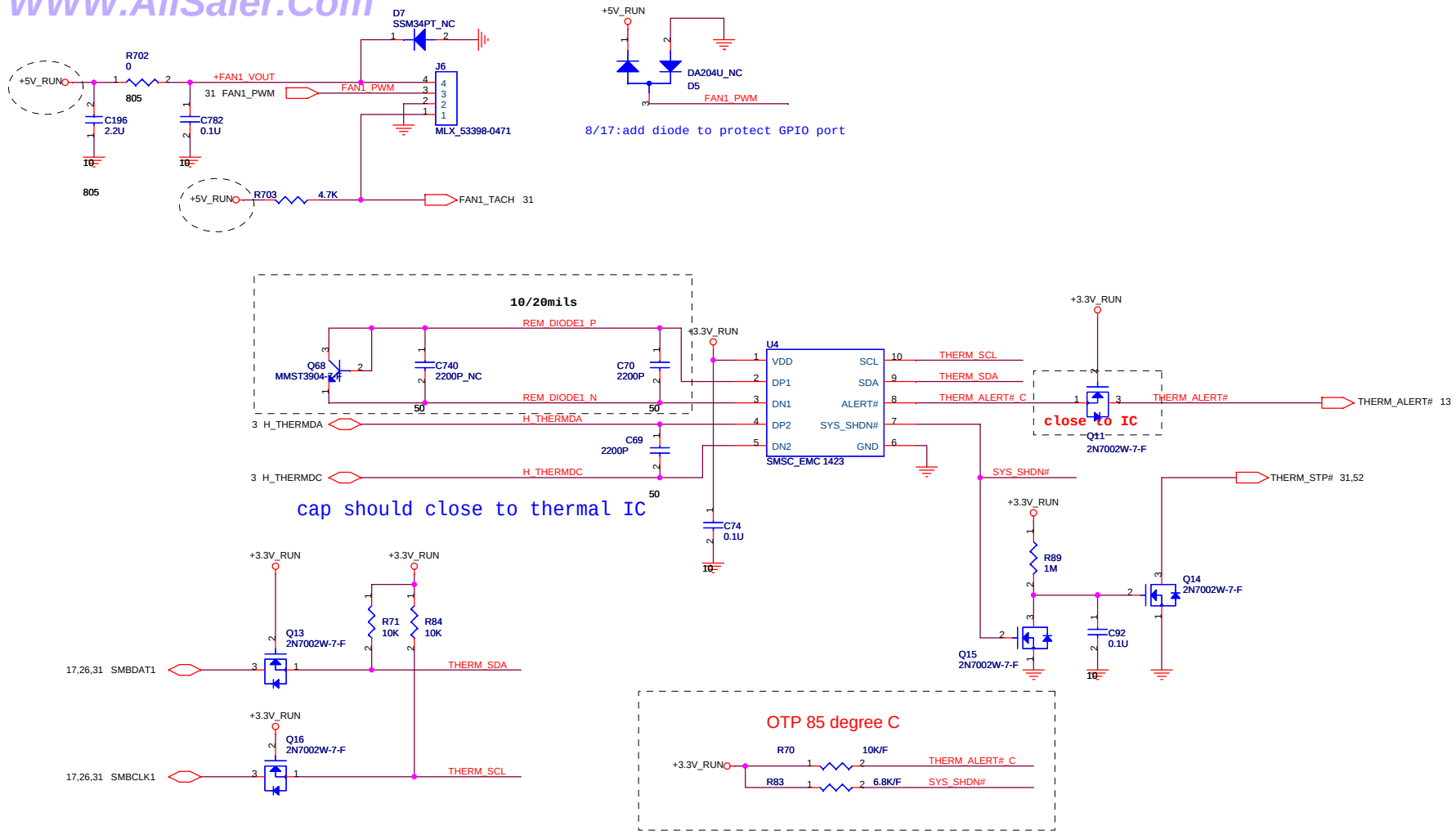

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Title	FAN & THERMAL	
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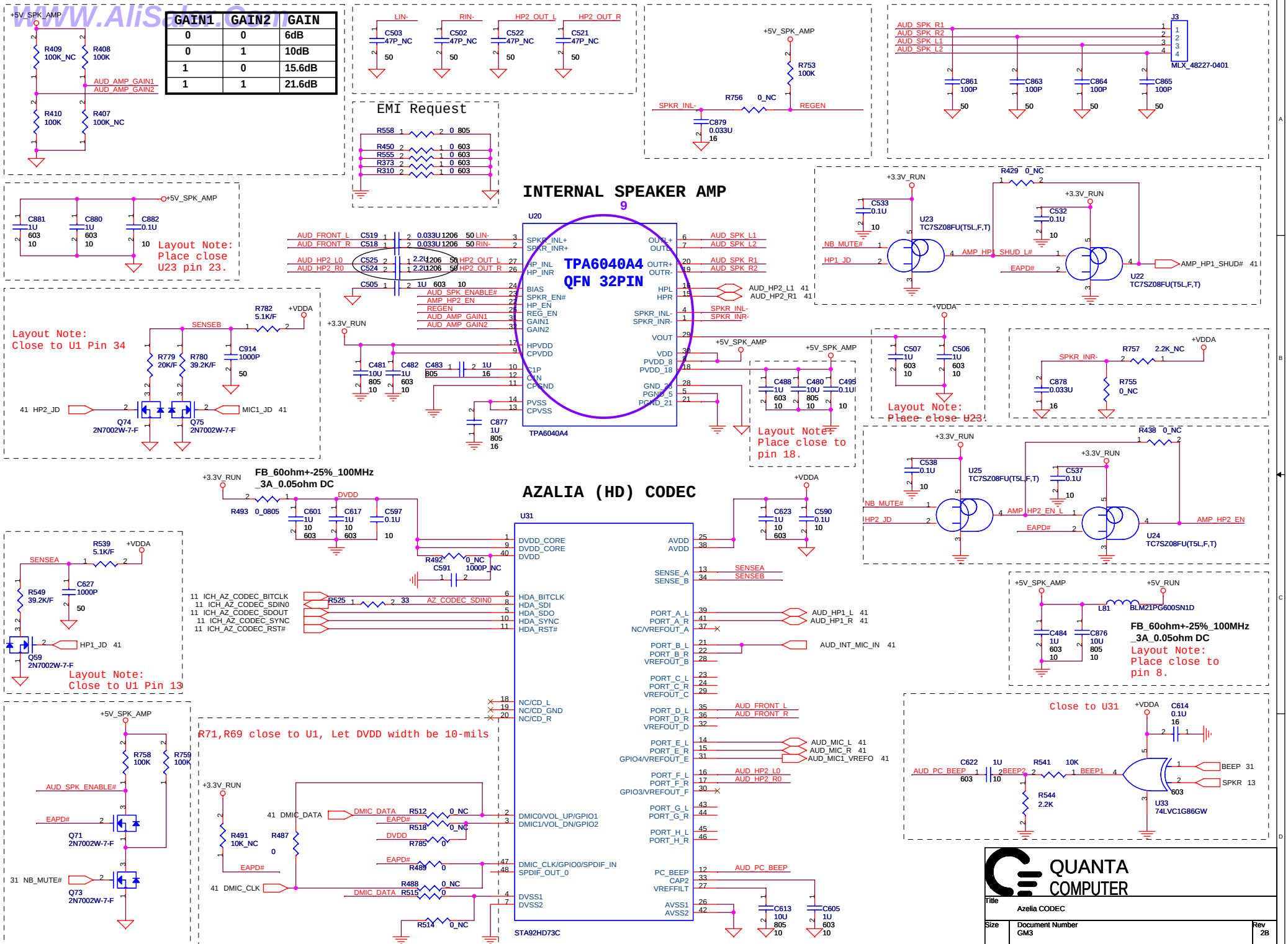
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



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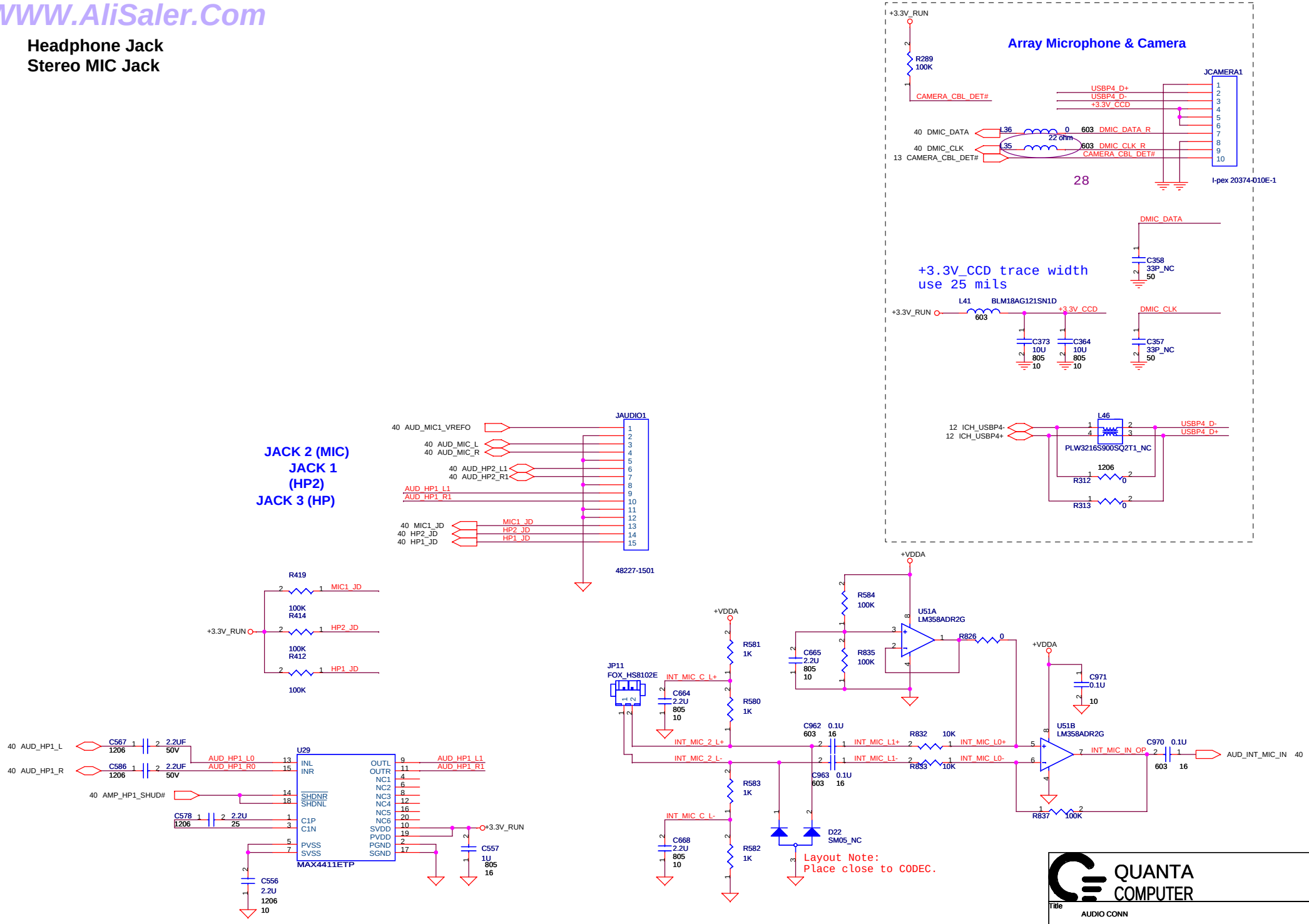
Headphone Jack
Stereo MIC Jack



Title	AUDIO CONN		
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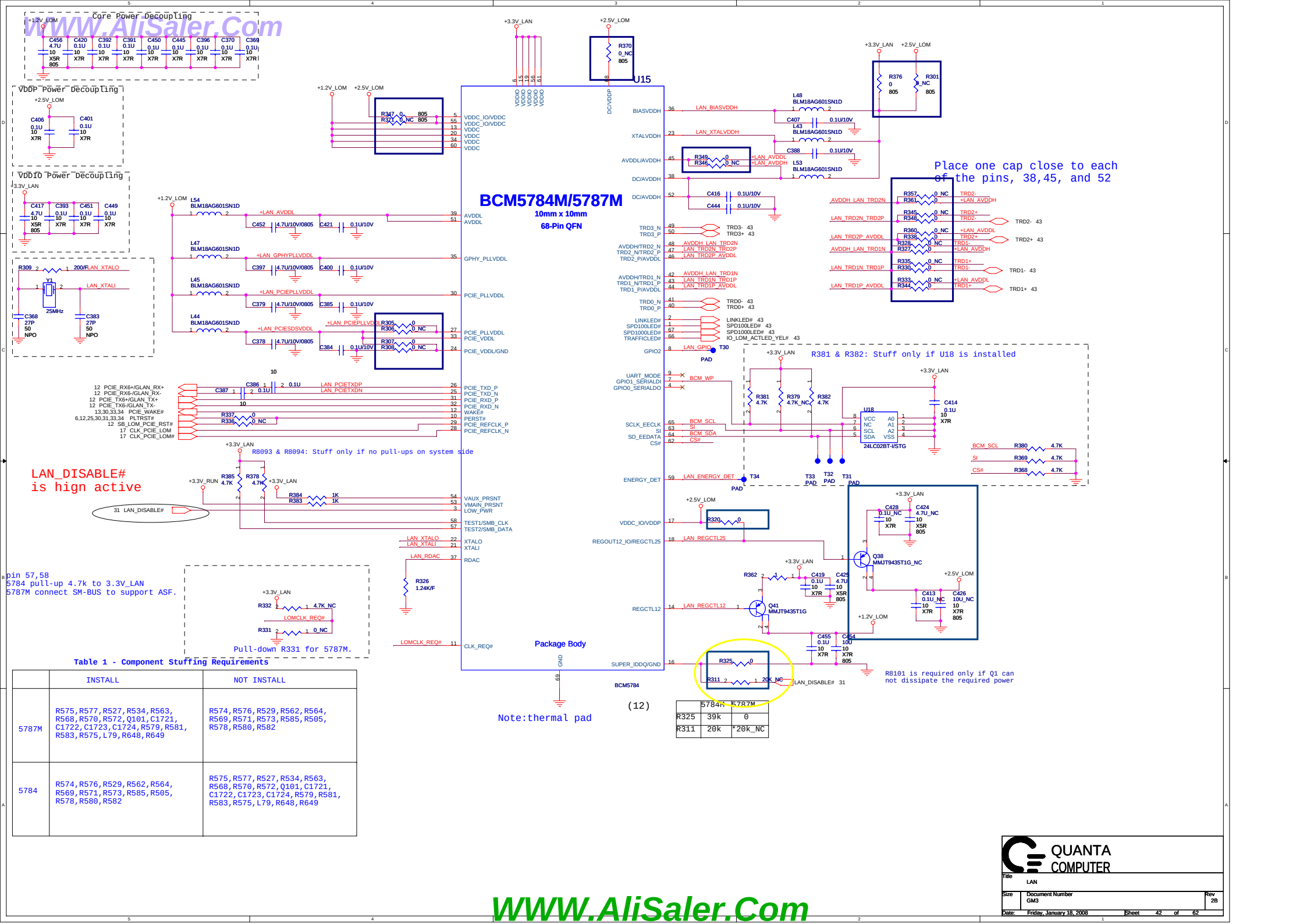

Table 1 - Component Stuffing Requirements

	INSTALL	NOT INSTALL
5787M	R575,R577,R527,R534,R563, R568,R570,R572,Q101,C1721, C1722,C1723,C1724,R579,R581, R583,R575,L79,R648,R649	R574,R576,R529,R562,R564, R569,R571,R573,R585,R505, R578,R580,R582
5784	R574,R576,R529,R562,R564, R569,R571,R573,R585,R505, R578,R580,R582	R575,R577,R527,R534,R563, R568,R570,R572,Q101,C1721, C1722,C1723,C1724,R579,R581, R583,R575,L79,R648,R649

	5784M	5787M
R325	39k	0
R311	20k	*20k_NC

QUANTA COMPUTER

Title: LAN

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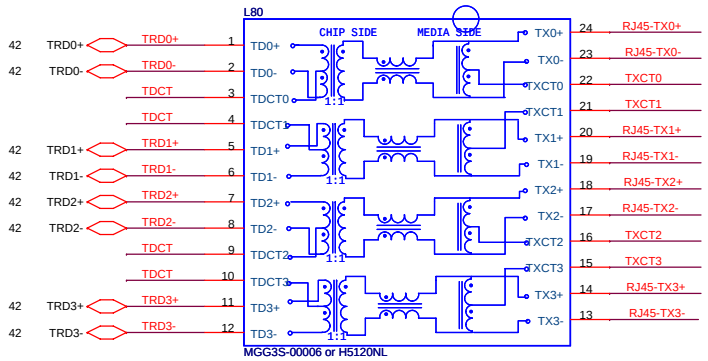
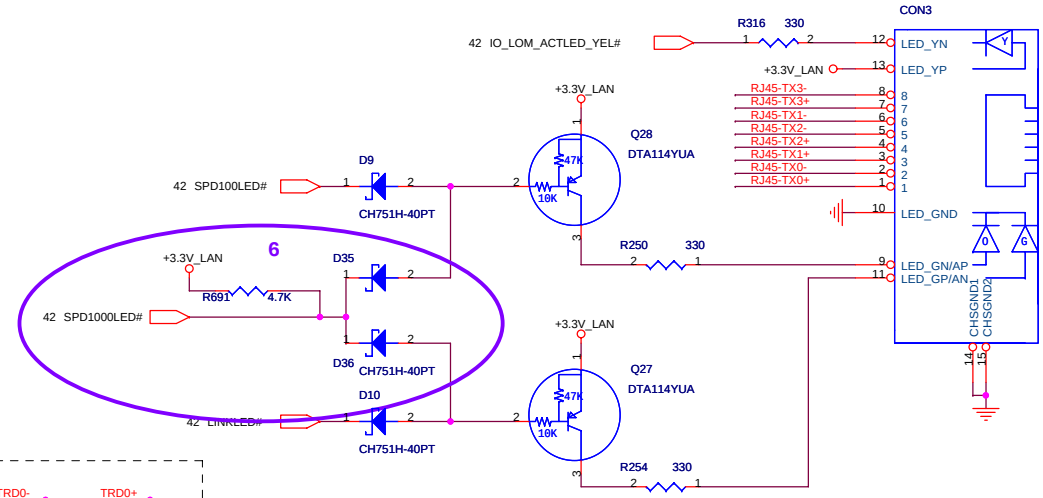
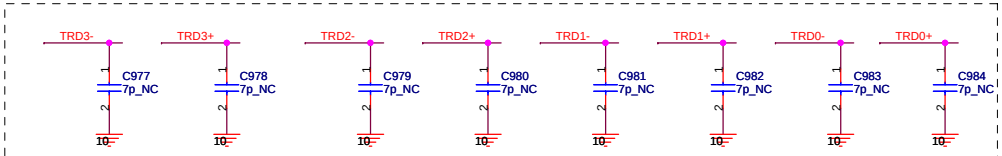
RJ-45 Connector

TRANSFORM

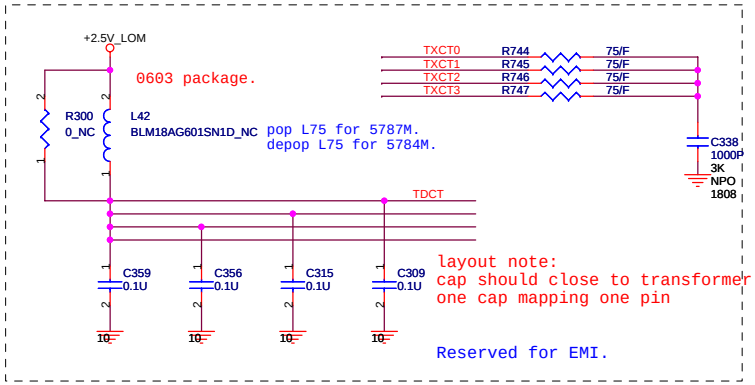


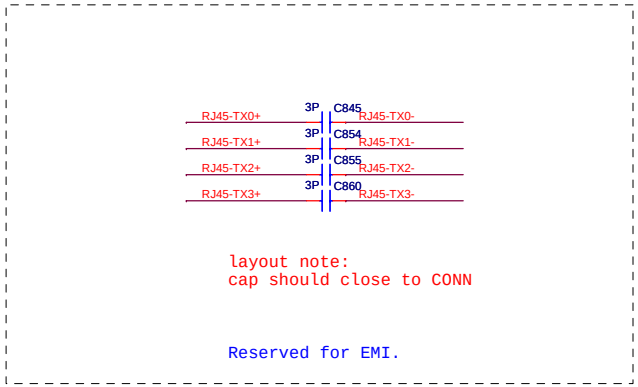




FOR EMI requirement and should close to L80

+3.3V_SUS
R317 0_0805
+3.3V_LAN





QUANTA COMPUTER

Title	LAN SWITCH	
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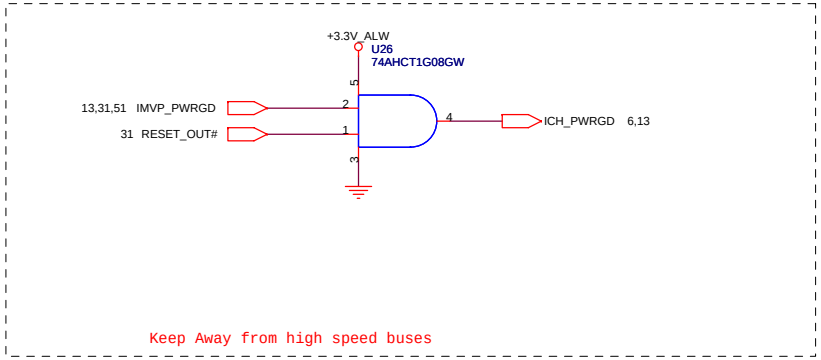

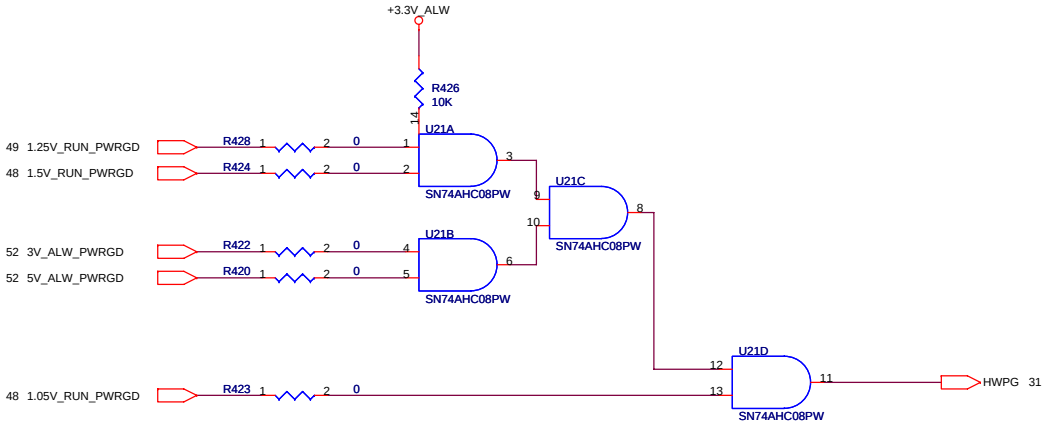

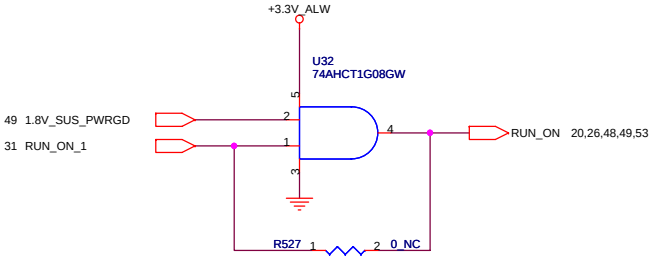

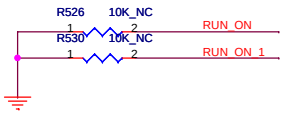

QUANTA COMPUTER

Title	System Reset Circuit
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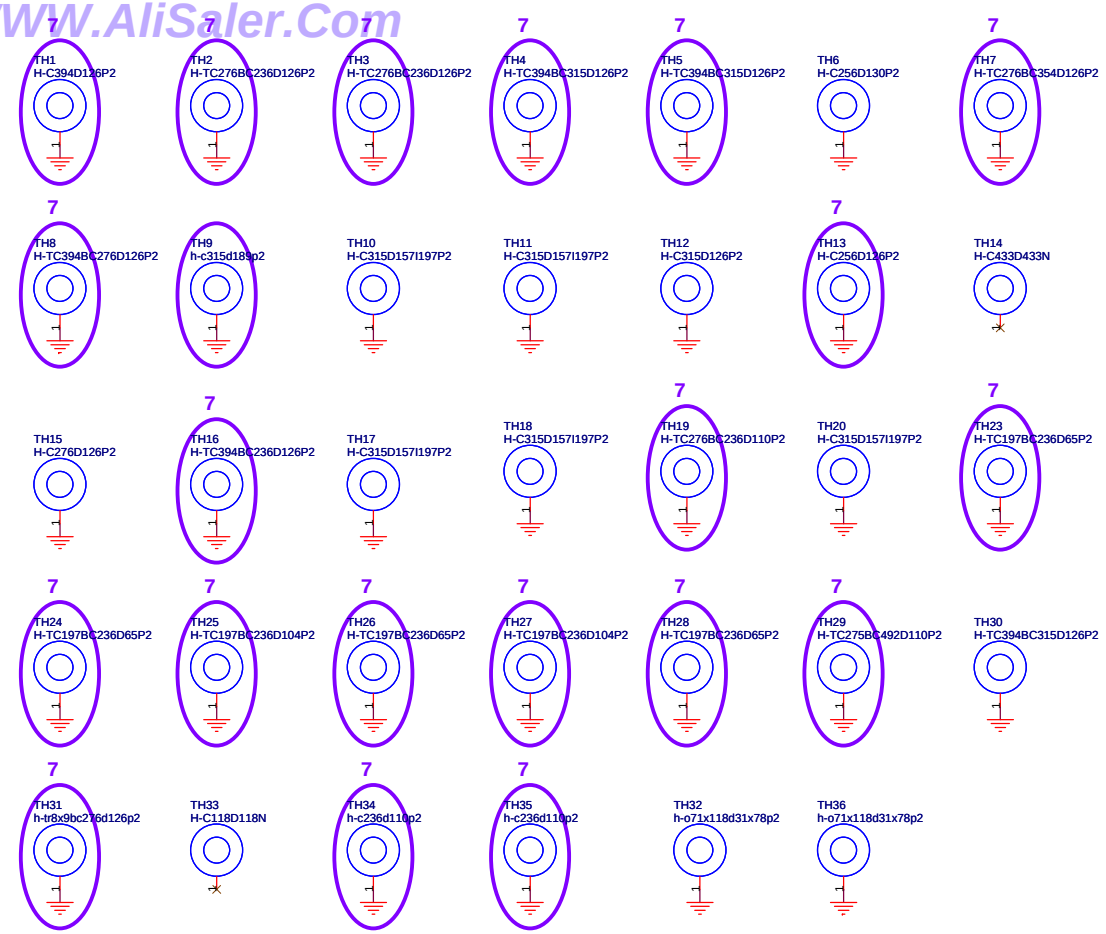

QUANTA COMPUTER

Title	Battery Selector
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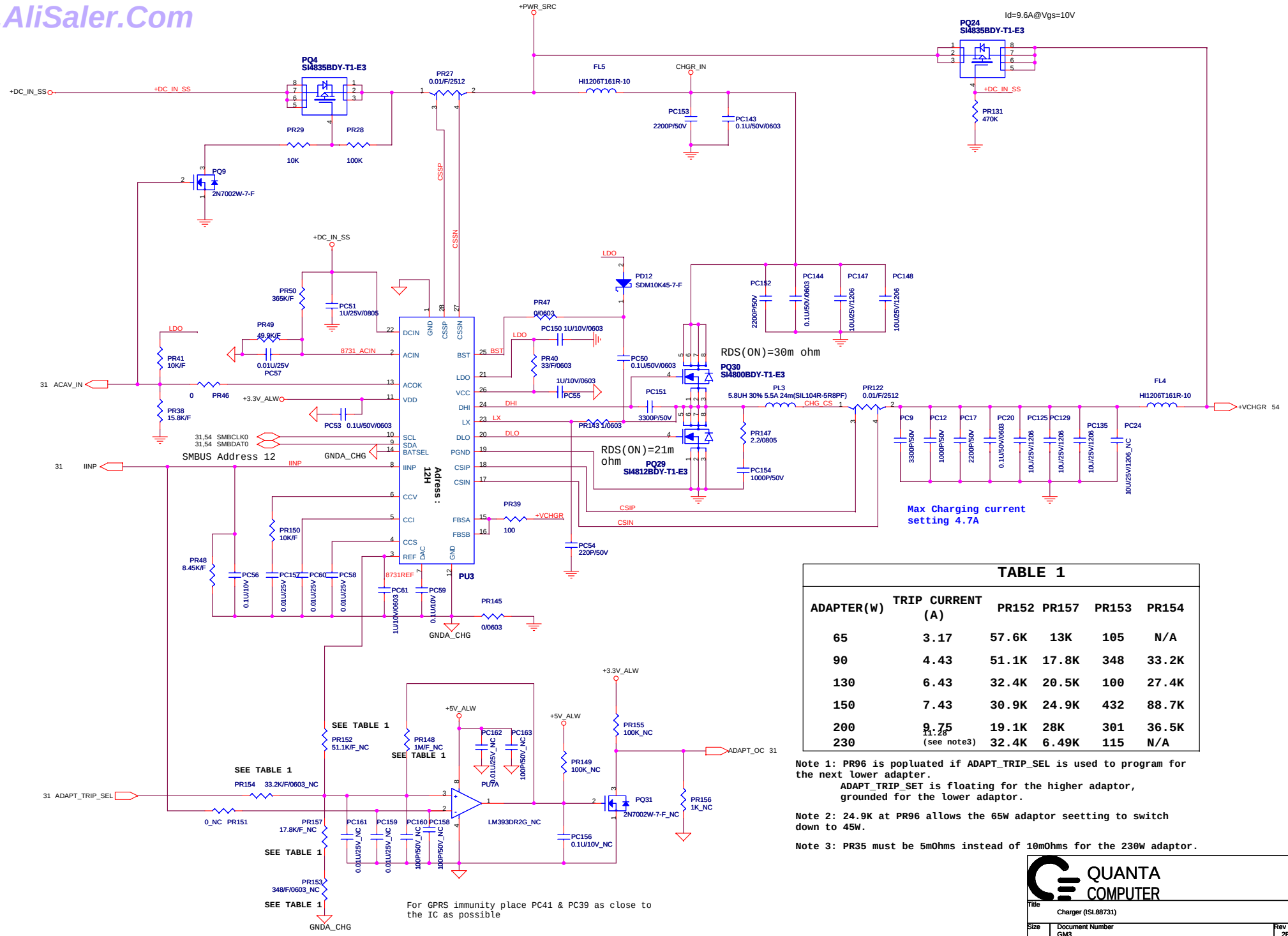

TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	PR152	PR157	PR153	PR154
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28 (see note3)	32.4K	6.49K	115	N/A

Note 1: PR96 is popluated if ADAPT_TRIP_SEL is used to program for the next lower adapter.
ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

Note 2: 24.9K at PR96 allows the 65W adaptor seetting to switch down to 45W.

Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.

QUANTA COMPUTER

Title	Charger (ISL88731)	
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Title		
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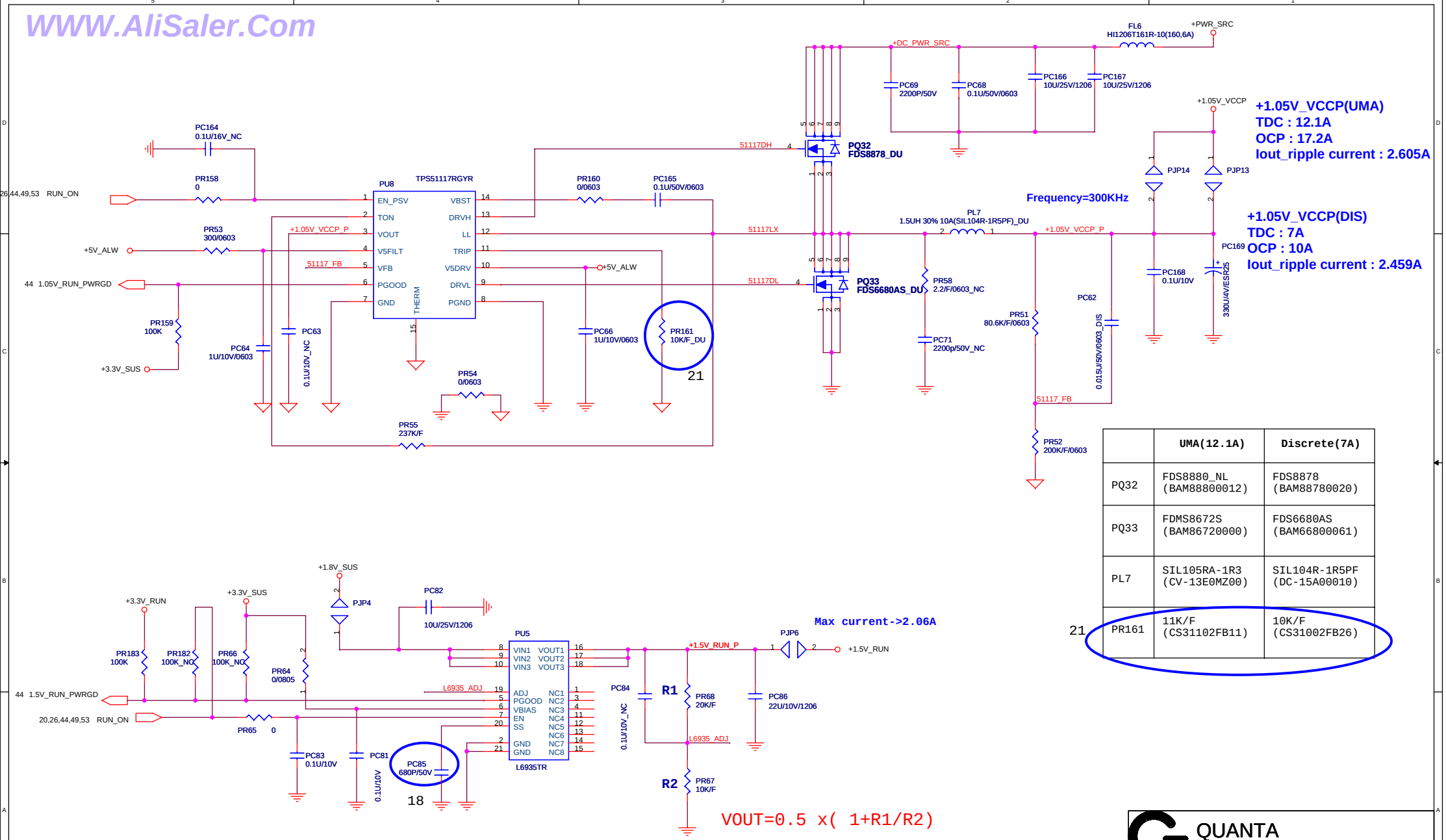

	UMA(12.1A)	Discrete(7A)
PQ32	FDS8880_NL (BAM88800012)	FDS8878 (BAM88780020)
PQ33	FDMS8672S (BAM86720000)	FDS6680AS (BAM66800061)
PL7	SIL105RA-1R3 (CV-13E0MZ00)	SIL104R-1R5PF (DC-15A00010)
PR161	11K/F (CS31102FB11)	10K/F (CS31002FB26)

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QUANTA COMPUTER

Title

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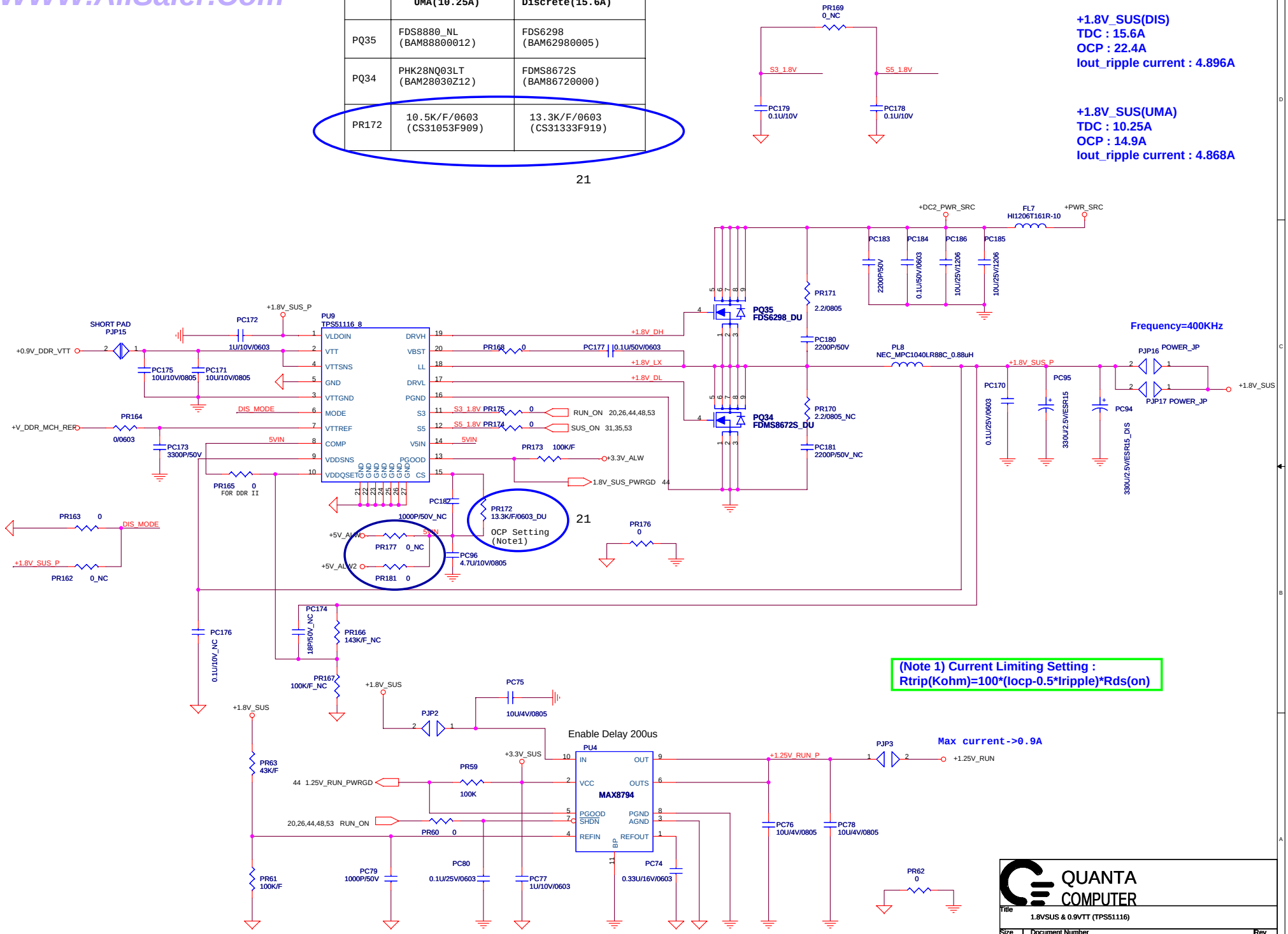
	UMA(10.25A)	Discrete(15.6A)
PQ35	FDS8880_NL (BAM88800012)	FDS6298 (BAM62980005)
PQ34	PHK28NQ03LT (BAM28030Z12)	FDMS8672S (BAM86720000)
PR172	10.5K/F/0603 (CS31053F909)	13.3K/F/0603 (CS31333F919)

21



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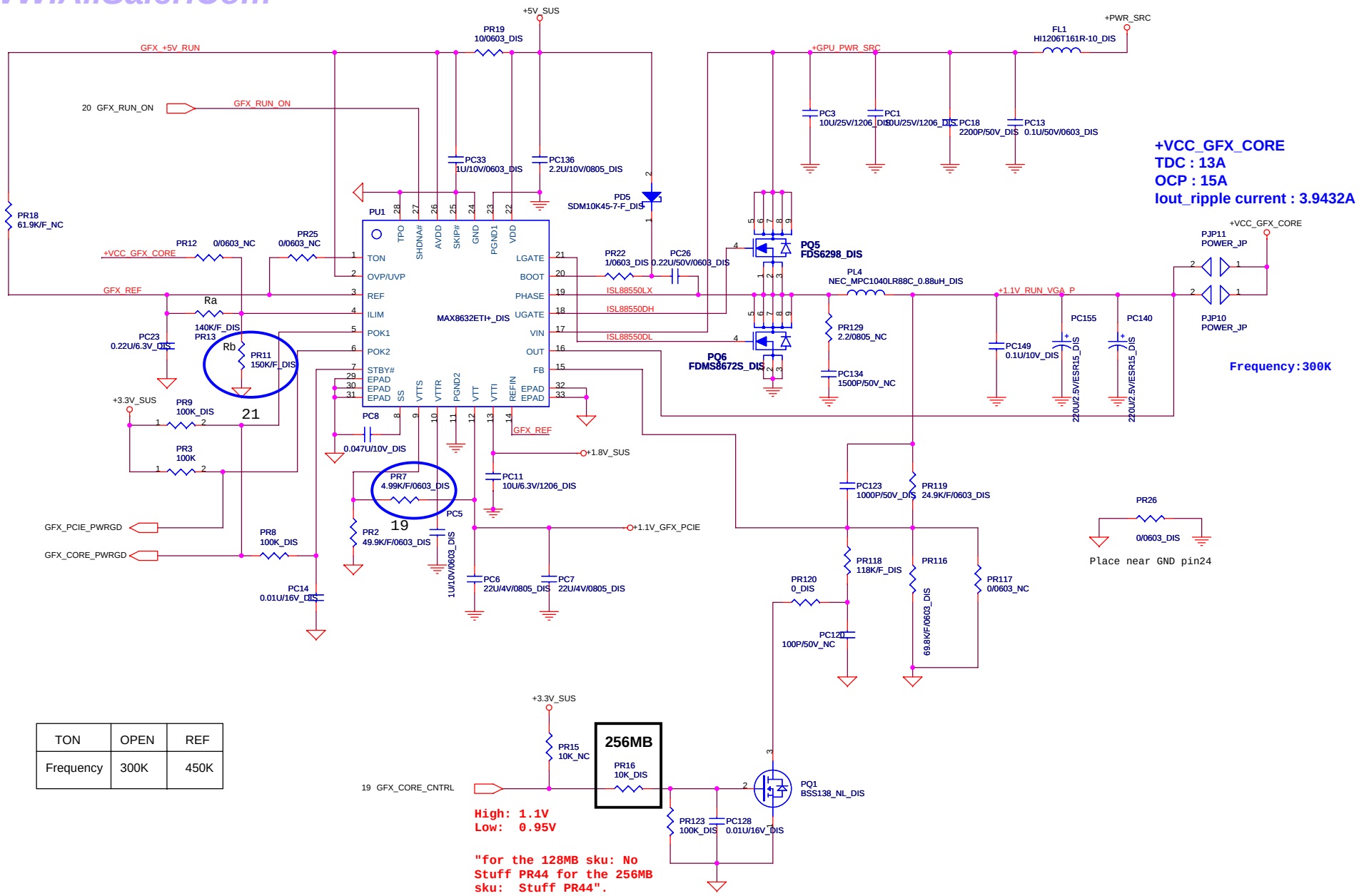

+VCC_GFX_CORE
TDC : 13A
OCP : 15A
Iout_ripple current : 3.9432A

Frequency:300K

TON	OPEN	REF
Frequency	300K	450K

ILIM	Iovp=(2*(Rb/(Ra+Rb))*0.1*(1/RDSON)+(I_DELTA/2)
SKIP#	AVDD = Low-noise, forced-PWM mode. GND = Pulse-skipping operation.
OVP/UVP	The overvoltage limit is 116% of Vout. The undervoltage limit is 70% of Vout.

QUANTA COMPUTER

Title	VGA DC/DC	
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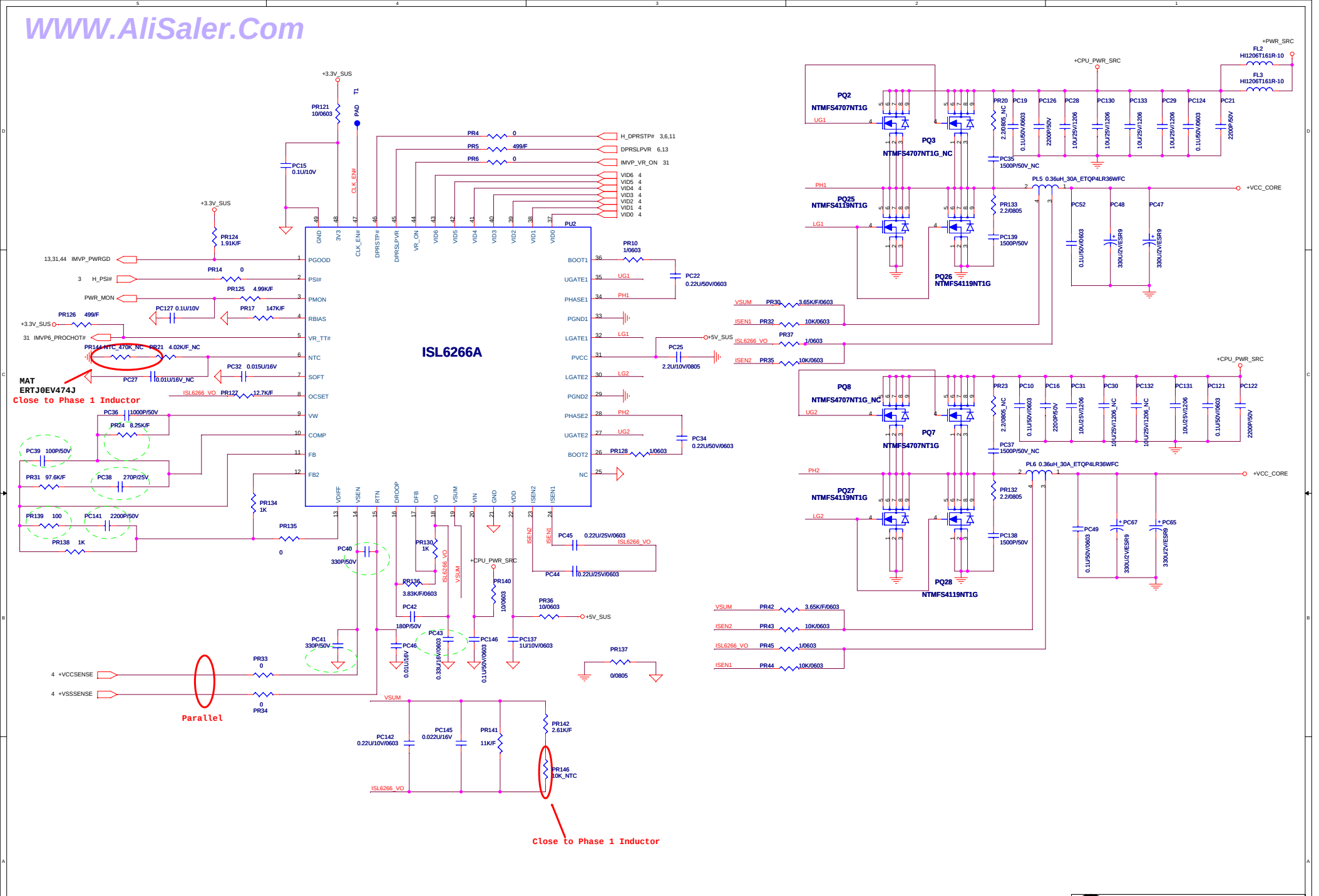

QUANTA COMPUTER

Title	CPU_Core_2Phase (ISL6266)	
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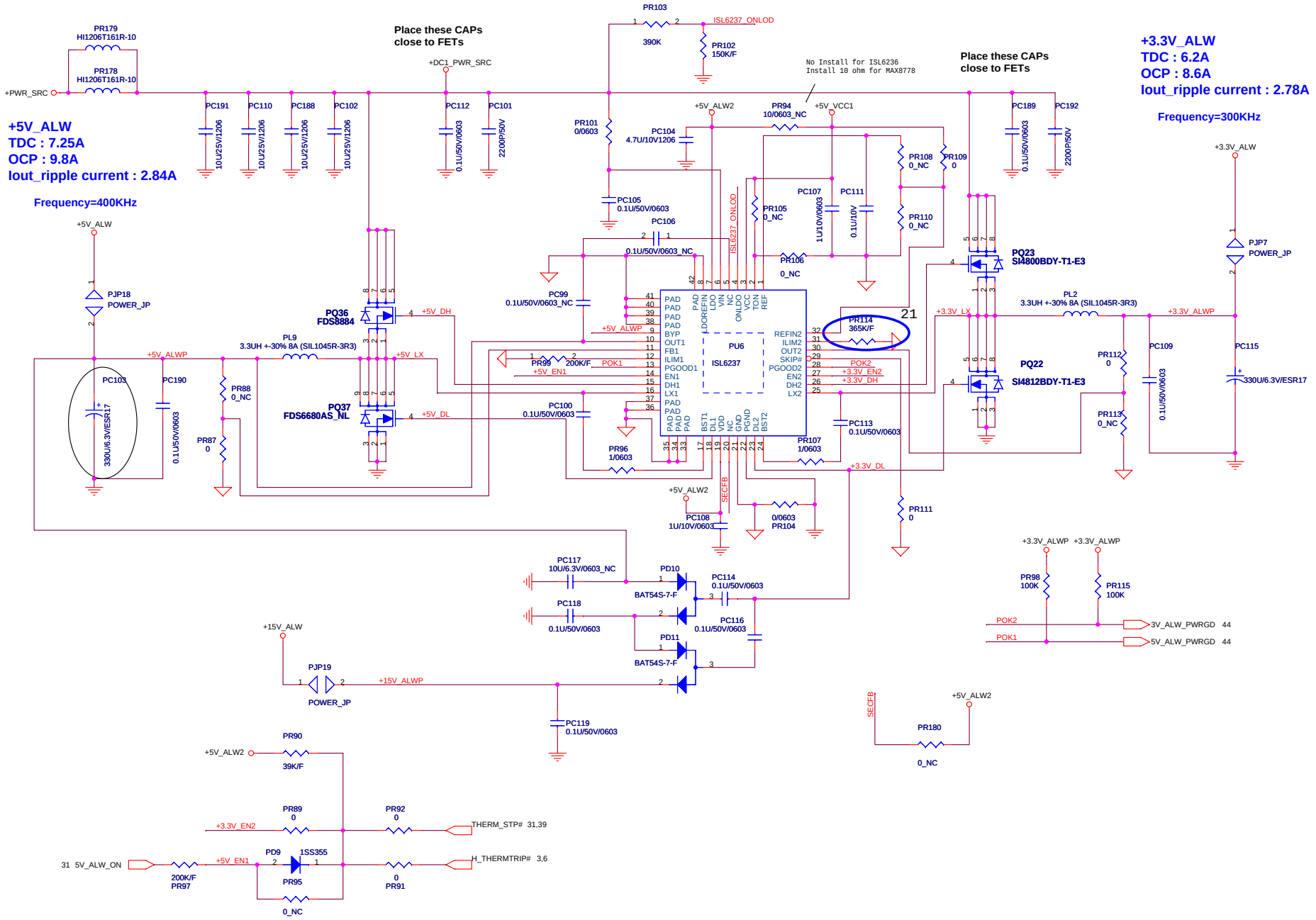
DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW



QUANTA COMPUTER	
Title	VGA DC/DC
Size	Document Number GM3
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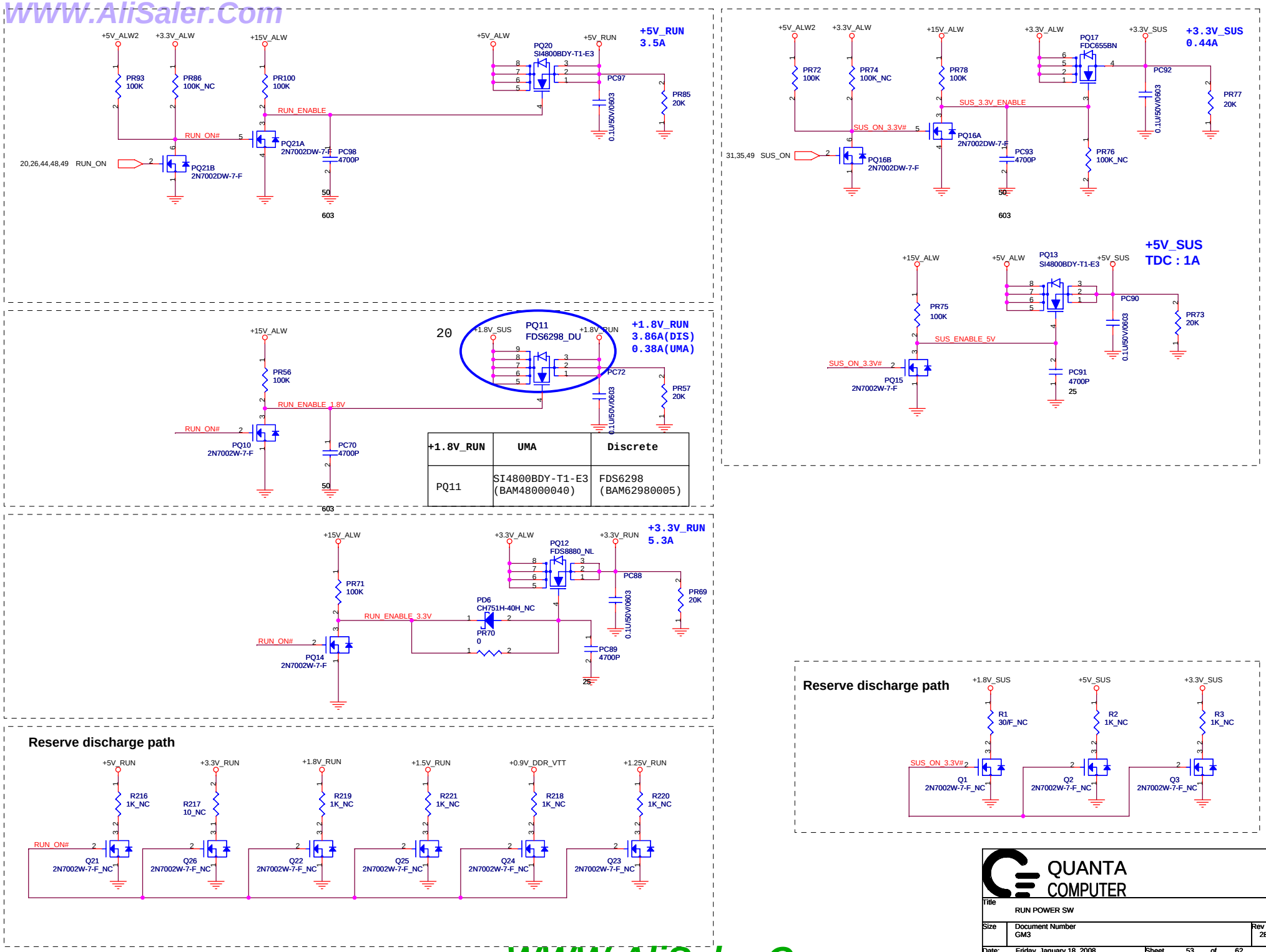

+1.8V_RUN	UMA	Discrete
PQ11	SI4800BDY-T1-E3 (BAM48000040)	FDS6298 (BAM62980005)

QUANTA COMPUTER

Title	RUN POWER SW
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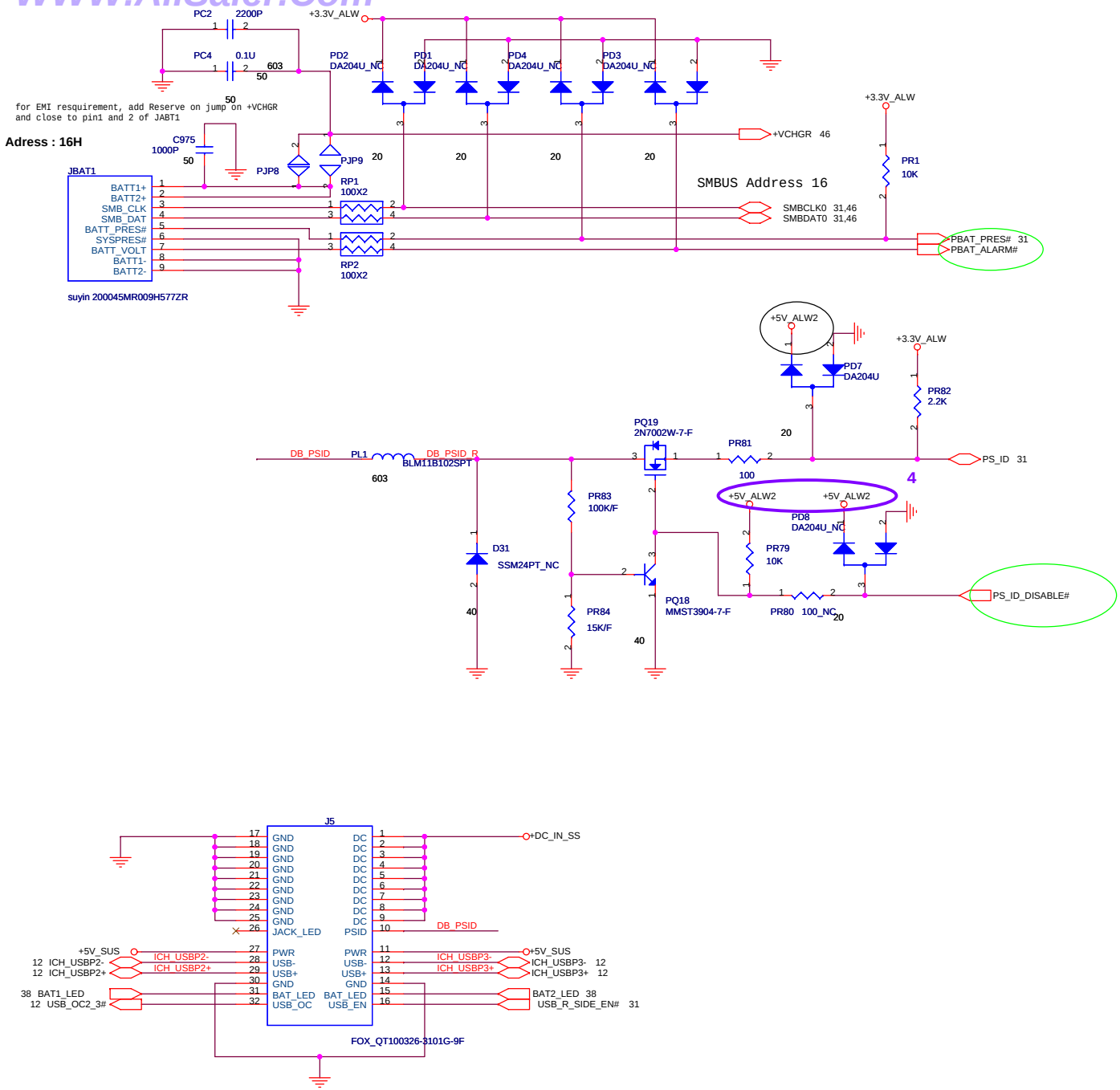

8/15: move the righT side USB and DC-in connector schematic to DB.
so change BTB(J14) CONN to 32pin

QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
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Reserved for EMI.

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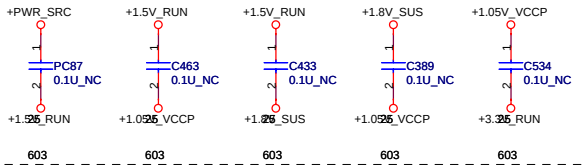
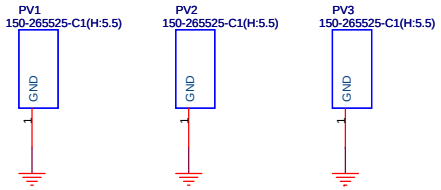
Stitching caps





Page 26
SATA (HDD&CD_ROM)

Page 27
PCCARD /CONN

Page 31
SIO(MEC5025)

Page 38
Azelia CODEC

Page 40
LAN(BCM5755M)

Page 48
1.5VRUN,1.05V(VTT)

Place C860,C216,C1426 close to PQ33.
Place C862,C222,C1427 close to PQ73.

Page 49
1.25V,1.8V,0.9V

Place C867,C254,C1428 close to PQ91.
Place C863,C253,C1429 close to PQ92.

Page 51
CPU_MAX8786(3phase)

Page 52
D/D Power

QUANTA COMPUTER

Title	EMI CAP	
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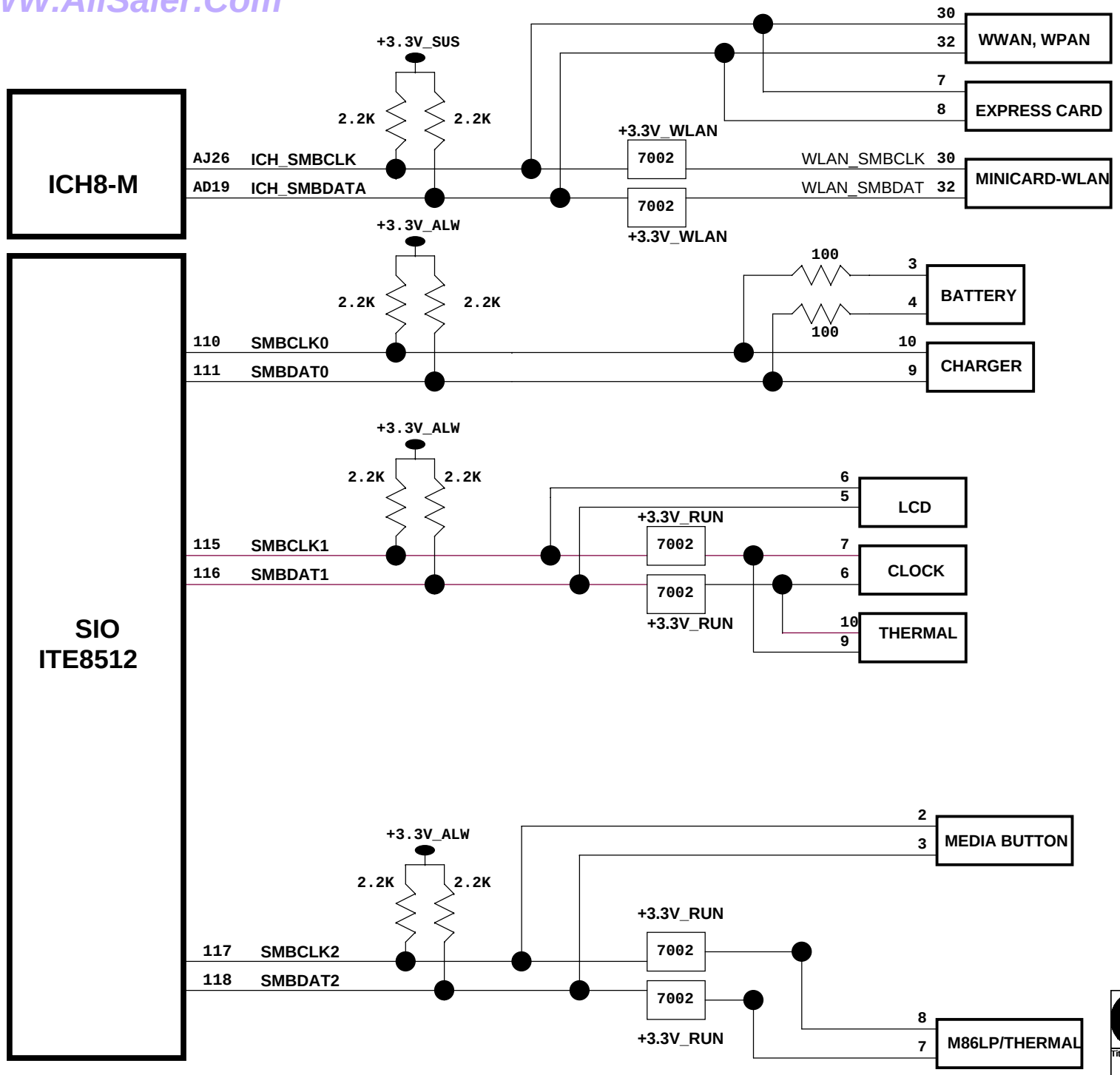

QUANTA COMPUTER

Title	SMBUS BLOCK
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH					
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH					
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH					
S5 (SOFT OFF) / M1	LOW	HIGH	LOW					
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH					
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH					
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW					

PM TABLE

State \ power plane	+3.3V_ALW +3.3V_RTC_LDO +3.3V_WLAN +5V_ALW +15V_ALW	+1.8V_SUS +1.8V_LOM +3.3V_LAN +3.3V_SUS +5V_SUS	+0.9V_DDR_VTT +1.05V_VCCP +1.25V_RUN +1.5V_CARD +1.5V_RUN +3.3V_CARD +3.3V_CARDAUX +3.3V_R5C832 +3.3V_RUN	+3.3V_RUN_CARD +2.5V_RUN +5V_MOD +5V_RUN +5V_SPK_AMP +CPU_PWR_SRC +VCC_CORE +VDDA	+DC_IN +DC_IN_SS +PWR_SRC +RTC_CELL
S0	ON	ON	ON		ON
S3	ON	ON	OFF		ON
S5 S4/AC	ON	OFF	OFF		ON
S5 S4/AC don't exist	OFF	OFF	OFF		ON

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
BCM4401B	AD16	REQ#0 / GNT#0	PIRQB
R5C833	AD17	REQ#1 / GNT#1	PIRQC: Card reader PIEQD: 1394

	USB PORT#	DESTINATION
ICH8-M	0	Right Top
	1	Right Bottom
	2	Side TOP
	3	Side Bottom
	4	Ext. USB TOP
	5	DIgital Camera
	6	Express Card
	7	WPAN/Bluetooth
	8	Ext. USB Bottom
	9	WWAN
ECE 5011	1	None
	2	None
	3	None
	4	None

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 WPAN
Lane 4	Express Card
Lane 5	None
Lane 6	None

QUANTA COMPUTER

Title	Schematic Block Diagram1	
Size	Document Number GM3	Rev 2B
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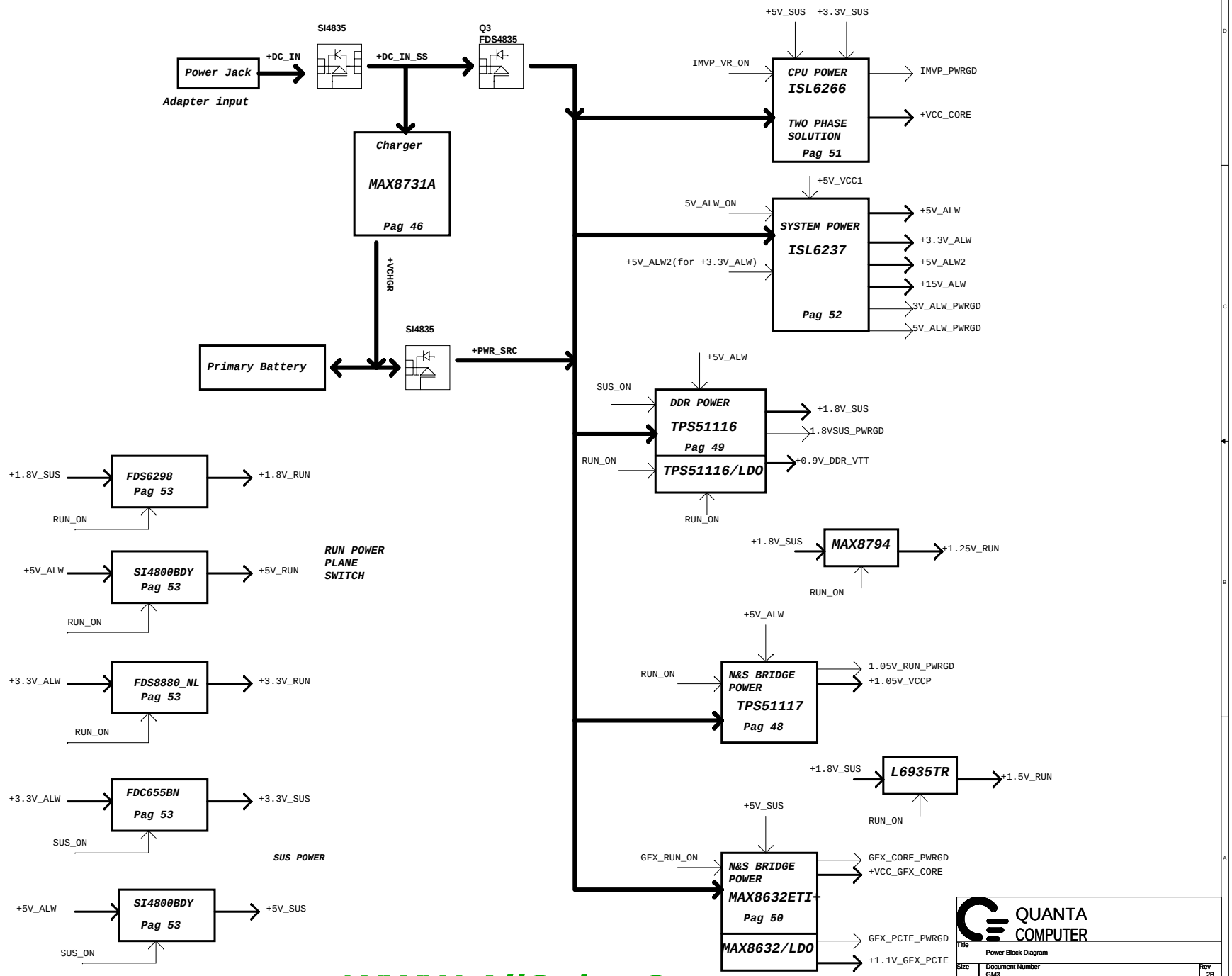
GM3 Power Design Block Diagram
2007/09/06



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Model	Item	Page	Date	Rev.	Description
Pacino of Intel	1	All	7/25	1A	Base on David.Lin 070725 1409 release preliminary schematic to check the all part PCB footprint. I found there are some parts not had footprint and update it. The change location as below. There are some concern need to highlight: 1. Discharged to CH751H-40PT. 2. LB8 & LB9 need to changed to 0ohm PTC part. 3. USB jack need to double check. 4. JKB1, JMDB1, JSP1,JI1B need to get the spec for create new layout footprint and apply for new P/N. 5. JDIM1 & JDIM2 should be combined to one JDIM. U12, L27, L28, C225, C226, D4, L9, U3, JDIM2, D1, LB4, LB5, U14, U18, U22, U23, U25, BT2, CON2, CON3, L34, L35, Q10, U11, U13,ESD1, CON7, D15, D38, D39, D40, JACMCR1, JKB1, JMOD1, JP1, L15, M1, Q7, Q67, SW1, U28, U41, FL1, FL3, FL4, FL7, FL8, FL9, FL10, FL11, JDC1N1, PC125, PC139, PC155, PC153, PC161, PL3, PL4, PL10, PL11, PL12, PQ13, PQ24, PQ42, PQ43, PQ44, PQ45, PR84, M11, M14, PU3.
	2	39	8/13	1A	FAE review schematic and recommend add CR456 & CR356 between MEM_DIODE1_P and MEM_DIODE1_N. This is just a reservation in case there's any noise coupling issue happening. Then have 2 different filter cap locations (one near EMC1423 and the oyher near the DTP 3904 diode) to try to reduce the noise. Of course, only one cap can be installed.
	3	25	8/13	1A	FAE review schematic and recommend add poly switch and 0.1u cap colse to 5V_RUN of HDMI CONN to avoid MB reboot.
	4	29	8/15	1A	FAE review schematic, NC FILO pin since SC833 don't need cap to GND
	5	19	8/15	1A	The strap on VIP[3] is for enabling HD Audio on MB6. so pull to hign.
	6	54	8/15	1A	move the right side USB and DC-in connector schematic to DB. so change BTB(J2) CONN to 32pin
	7	19	8/15	1A	8/15 FAE review schematic: reverse TMDS signal for working property. change voltage allocation resistor to make sure the input clock swing level is at 1.8V
	8	39	8/16	1A	8/16:per SPEC recommend: use 7002 to avoid the leakage current from 3V_SUS.
	9	37-39	8/17	1A	8/17:add diode to protect below GPIO port,p39---FAN1_PWM p38---SNIFFER1 and POWER_ SW_IN0#, p37---MEDIA_INT
	10	52	8/20	1A	8/20: For FAE suggestion. Charge pump from +5V LDO, might cause high ripple voltage. Add PC116 10U/6.3V/0603.
	11	52	8/20	1A	Since FDS8878 Rg too big,change PQ44 to FDS8884.
	12	52	8/20	1A	Change PR225 to 180K and PR224 to 294K for setting current limit.
	13	52	8/20	1A	For FAE recommend , PD16 could be deleted.
	14	49	8/20	1A	Change PR85 to 143K for 1.82 output voltage
	15	48	8/20	1A	Due to output ripple current too big ,cheange PL25 from 0.88uH to 1.5uH.
	16	48	8/20	1A	PR449 should be cancelled, not necessary
	17	48	8/20	1A	Change PR452 to 9.09k for OCP
	18	48	8/20	1A	For FAE recommend. PC447 no stuff, reserved.
	19	48	8/20	1A	Add PC78 for meet output ripple current.
	20	48	8/20	1A	Change PR182 to 4.53K and PR185 to 49.9k for setting VTT=1.1V. (VTTS =REFIN/2=1V)
	21	38	8/22	1A	Added LED level shift for support white LED need used 5V drive.
	22	22	8/23	1A	add level shift circuit to protect thermal IC
	23	42	8/23	1A	add level shift circuit to provent ALW and LAN plan interconnect
	24	13 31 37 40 48 55	8/24	1A	Check single net and correct by JM
	25	52	8/27	1A	Due to SIL1045R-3RBPF will be EOL, change PL11,PL12 to SIL1045R-3R3.
	26	37	8/27	1A	change KB pin number to 32 pin
	27	43	8/28	1A	change LED of LAN jack control signal to LINKLED
	28	43	8/28	1A	Co-layout SIM card connector and WTB together
	29	37	8/28	1A	Dell had update K/B pin define to 34 pin and re-define pin definition
	30	31	8/28	1A	KSO18 is output pin, so change to pin B5, and KB_DET# from pin B5 change to pin 70.
	31	39	8/28	1A	reverse 1-4 pin definitiom for thermal team design
	32	28,12	8/29	1A	change RSc833 PCI_PIRQD# to PCI_PIRQB# for AMD platform signal control requirement
	33	37	8/29	1A	due to move keyboard light sensor to media button board, add KB_BACKLITE_SET function to media button connector pin 10.
	34	37	8/29	1A	change keyboard pin number to 32 pin
	35	48	8/29	1A	For Dell recommend,change 1.5V LDO from MAX8794 to ST L6935.
	36	49	8/29	1A	For TI FAE recommend,connect PC76 to GND.
	37	35	8/30	1A	For support power USB function, change power to 5V_ALW
	38	31	8/30	1A	change IMVP6_PROCHOT# from pin B8 to GPI 1 for design requirement. and pinB8 assign to 5V_ALW_ON
	39	25,43,38	8/30	1A	for EMC team requirement, reserve cap, ESD protect, common choke at CON side
	40	52	8/30	1A	Add PC180 for reserve MAX8778 IC.
	41	52 53	8/30	1A	Due to Pacino need to support USB charger function,change following item. 1.Change power plan from +5V_ALW to +5V_ALW2:pin9 ,pin7,pin19, PC116 and PR156 2.Add a load switch PQ42 for +5V_ALW to +5V_SUS
	42	28	8/31	1A	refer MB8 platform, change to 100 ohm
	43	22	9/2	1A	Reserve external spread spectrum circuit for ATI graphic using
	44	48	9/3	1A	change PR455 to 237K from 178K to setting switching operating frequency at around 300 KHz
	45	52	9/3	1A	For FAE recommend, change PD14 input power from "+5V_ALW2" to "+5V_ALW" and PC116 can be NA.
	46	52	9/3	1A	For FAE recommend, connect pin20 to pin19 for ISL6236 (or MAX8778) can populate on ISL6237 location.
	47	49	9/3	1A	Change PC155 to correct net name "+1.8V_SUS_P".
	48	20	9/3	1A	MB6 internal thernal protect function pin is high active, re-design protect logic circuit for it.
	49	54	9/3	1A	for EMI requirement, add Reserve on jump on +VCHGR and close to pin1 and 2 of JABT1
	50	38	9/3	1A	Reserve ESD protector at J4 pin1 (+3V_RUN)for Biometric (close to J4)
	51	46	9/3	1A	Add PC39 for reserve debug noise issue.
	52	48	9/3	1A	Change PU5 pin6 through PR58 to +3.3V_SUS.
	53	49	9/3	1A	Change PR79 from 10K to 0ohm.
	54	50	9/3	1A	For reserve EMI sunnber, add PR157 and PC117.
	55	48	9/3	1A	For DELL recommend , reserve PC143 and PC144 for TI controller.
	56	38	9/3	1A	For DELL recommend , Add GPIO pin to mask HDD and BT LED active
	57	17,33,34	9/3	1A	for WLAN card using CLK-REQ pin, so change CLK_PCIE_MINI1 to WLAN and CLK_PCIE_MINI3 to WPAN.
	58	26,6	9/3	1A	add third pair LVDS signal to support 24bit panel
	59	31	9/4	1A	delete JACK_LED_DET# pin for DC jack design, so move KSO18 to pin99.
	60	46	9/5	1A	Reserve a 0 ohm PR59 resister for EA test.
	61	48	9/5	1A	Add PC145 for ST FAE recommend.
	62	37	9/6	1A	Add KB_BACKLITE_EN control circuit on MB side
	63	37	9/6	1A	Add 3_ALW at pin 5 for Lid switch IC power pin
	64	42	9/6	1A	Reserved BCM5784M SUPER_IOOQ circuit.
	65	30	9/8	1A	add MMC card function at card reader connector

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Model	Item	Page	Date	Rev.	Description
Pacino of Intel	1	12,13, 17,25, 60	9/27	2A	modify SST design issue. 1. delete unnecessary 0 ohm resistor 2. select correct frequence for DIS/UMA(R351&R342) 3. CARD_CLK_REQ0 pull high 4. PLTRST_DELAY# pull down to avoid floating. 5. NC R451 to set Boot BIOS Strap for LPC interface
	2	52 ,50	10/2	2A	For second source concern, change below item. 1. Change PD9 from BAS316 to 1SS355 2. Change PD5 from CMS01H-40PT to SDM10K45-7-F 3. Change PQ1 from BSS138-7-F to BSS138_NL
	3	8	10/3	2A	use 0805 0 ohm to instead of jump(1/8W, 1.6A per resistor)
	4	19	10/3	2A	pull high the GPIO 0 & GPIO 1 to enable PCIE FULL TX OUTPUT SWING and PCIE TRANSMITTER DE-EMPHASIS function to solve no display problem.
	5	41	10/15	2A	The camera pin assignment changed : 2 pin camera power pin and they are 3.3 V ..
	6	40	10/15	2A	change resister setting for STA92HD73C chip
	7	46 52	10/15	2A	Due to SI4810BDY-T1-E3 will be EOL, change PQ29 and PQ22 from SI4810 to SI4812.
	8	19	10/16	2A	Due to VDDR4 and VDDR5(option reference source voltage) use 1.8V_RUN, FAE suggust DVPDATA use 1.8V pull high
	9	33	10/17	2A	remove external SIM card CONN that on MB side
	10	13	10/17	2A	It is multi_function pin(SMBALERT#/GPIO11). Before bios programming, the PIN function is SMBALERT.If it is pull high to 3.3_RUN, the ICH8 will be alert by this pin. It cause the S3 can't normally sleep when system cold boot first time. so change to SUS power
	11	38	10/18	2A	Sniffer behavior is reverse, so modify design at PT stage
	12	42	10/18	2A	change to 5784 design
	13	40	10/22	2A	change TPA6040A4 symbol design to meet SPEC definition
	14	19	10/22	2A	FAE suggust: Ground R28/G2B/B2B and Implement R2SET to GND even if DAC2 is unused.
	15	43	10/23	2A	for factory requirement---increase pad length for SMT yield rate
	16	41	10/24	2A	for DELL SPEC---change camera conn pin definition
	17	31, 37	10/25	2A	modify LED Key board Illumination schematic and remove EC pin 68
reserve	18	44	10/29	2A	HWPG monitor change: change 3V/5V_ALW_PWRGD to GFX_PCIE/CORE_PWRGD
reserve	19	12,13, 14,31	10/29	2A	create +3.3V_S5 and +5V_S5 power at ICH part to fix ITE chip SUS resume problem, and move LID_SW# to pinj 68 and pin 120 for S5_ON using
	20	35	10/30	2A	add FSUSB31KBX to control USB signal can be passed above SUS, and USB_SIN_SIDE_EN# can control whether USB can supply power for external device at S5 mode
reserve	21	53	10/30	2A	For EE request , add two power rail "+3.3V_S5" and "+5V_S5" for south-bridge battery mode.
	22	48	10/30	2A	1.5V_RUN_PWRGD pull-high to RUN_ON for solve glitch issue.
	23	38,54	10/30	2A	add 1000p cap and close to connector for EMI
	24	35	10/30	2A	change LCD connector pin definition for LED panel: 1. change pin 8 fore GND to +5V_ALW 2. change pin 16 from GND to LCD_VCC
	25	31	11/1	2A	change GPIO design 1. delete pin 83 SNIFFER_YELLOW# 2. move 5V_ALW_ON to pin 83 3. swap pin 108 WIRELESS_ON/OFF# and pin 35 SNIFFER_PWR_SW#
	26	38	11/1	2A	change GPIO design 1. swap WIRELESS_ON/OFF# and SNIFFER_PWR_SW# 2. remove SNIFFcircuitFER_YELLOW#
	27	31	11/5	2A	change GPIO design for fix thermail no function issue 1. NC ADAPT_OC and ADAPT_TRIP_SEL 2. add #V_ALW_ON function at pin 76
	28	3	11/5	2A	Modify H_THERMTRIP# Voltage Level shift circuit.
	29	41	11/6	2A	add one GND pin for Audio precision dB value
reserve	30	37	11/8	2A	add circuit to control CIR power
	31	49	11/12	2A	Add PR181 for reserve +5V_ALW2.
	32	43	11/12	2A	for EMI requirement, add 7p cap close to LAN switch
	33	37	11/13	2A	for DELL requirement, add fuse between +5V_RUN and +KB_LED
	34	31	11/13	2A	use pin 14(WRST#) to monitor THERM_STP# function
	35	25	11/13	2A	for Silicon image FAE suggestion: 1. EMI may come from the impedance mis-match, that'll get distorted waveform . Try to replace the common choke with (i.e 22 ohm) resistor; 2. Try to reduce the source termination resistor (i.e 300 ohm --> 150 ohm) to get cleaner eye . 3. change AVCC33V to 3.3V_RUN
	36	25	11/13	2A	per FAE suggestion:change C525 and C524 to 2.2u for batter Audio precision
	37	50	11/13	2A	Chnage PR11 to 100Kohm for set correct O.C.P.
	38	50	11/13	2A	For EE request, set VGA voltage to 0.95V/1.1V. Change PR116 to 69.8K and PR118 to 118K.
	39	4	11/13	2A	Base on acoustic team test ,add two EC-cap for noice issue. Stuff C733 and C766.
	40	52	11/13	2A	Base on test result, change PR114 to 294K for set OCP.
	41	48	11/13	2A	Change PR161 to 11K for set correct OCP.
	42	48	11/13	2A	For 1.05V jitter issue, chnage below item. UMA: Change output CAP from 390U/2.5V/ESR10 to 330U/4V/ESR25 Discrete: 1. Change output CAP from 390U/2.5V/ESR10 to 330U/4V/ESR25 2. Add PC62 1500PF
	43	48	11/13	2A	Change 1.05V UMA PQ33 from FDS6676AS to FDMS86725 for improve efficiency.
	44	49	11/13	2A	Base on EA report test , stuff PR171 and PC188 for reduce hiogh side VDS ring.
	45	46	11/13	2A	Due to software support UL function via "IINP", no stuff UL circuit.
	46	13	11/14	2A	add 4.7k on PCIE_MCARD1_DET# trace to solve WLAN card detect issue
	47	19	11/15	2A	change GPIO pin from 3.3V_RUN to 3.3V_delay to solve leakage problem between 3.3V_RUN and 3.3v_delay(4ms) when boot.

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Size: ECO change list

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Model	Item	Page	Date	Rev.	Description
Pacino of Intel	1	32	11/26	2B	Change RTC connector because ME modifyr.
	2	31	11/26	2B	Exchange 'SNIFFER_PWR_SW#' AND 'WIRELESS_ON/OFF#. per EC limition.
	3	31	11/26	2B	Change NUM_LED# from SIO pin98 to pin 88 and used Pin 98 for BID only per EC limition.
	4	54	11/26	2B	Change PSID relation parts to +5V_ALW2 for power saving in S5.
	5	38	11/26	2B	Change Sniffer Switch power rail from RUN plane to ALW plane.
	6	43	11/26	2B	Added LINK1000# for BCM cann't support GLAN LED drived by LINKLED#/SPD100LED#.
	7	45	11/27	2B	Modify Screw hole base on ME update.
	8	17	11/29	2B	Link to MCH DPLL clock is wrong. Change to correct link.
	9	31	11/30	2B	Fine tune GPIO define for EC.
	10	37	12/04	2B	Change MMB LED power source from 5V_ALW2 plane to 5V_ALW for power saving and avoid LED flash when AC in.
	11	22	12/04	2B	Check AMD +3.3V_DELAY power plane connection component for AMD new update REF133-7 file.
	12	40	12/19	2B	Change Audio AMP thermal PAD leave to NC.
	13	31	12/26	2B	Change SMBus pull hihg resistor form 2.2k to 10k for LED panel flash.
	14	37	12/26	2B	since we will use WLAN and BT LED to show function at factory side. Change power supply of Cap and Num LED from 5V_ALW2, 3.3V_ALW to 5V_RUN and 3.3V_RUN.
	15	19	12/26	2B	Change HDMI detect circuit to solve external panel feed back voltage shortage then caude ATI chip can't switch to HMDI mode problem.
	16	37	12/26	2B	Change the Media board power from 3V_ALW to 5V_ALW2 to solve LED flash issue when AC/Bat plug in.
	17	37	12/26	2B	Change the lid switch IC power source from 3.3V_SUS to 3.3V_ALW to avoid system can enter S4 mode but wake up fail problem
	18	48	1/3	2B	Change PC85 to 680P for meet sequence.
	19	50	1/3	2B	Change PR7 to 4.99K for adjust +1.1V_GFX_PCIE rail.
	20	53	1/3	2B	Change PQ11 from SO8 to power package footprint.
	21	48 49 50 52	1/3	2B	Change PR161 ,PR172 ,PR11 ,PR114 to correct resistance for reliability request.
	22	35	1/4	2B	remove USB charge circuit
	23	26	1/7	2B	pull DPST signal to high for setting 100% duty cycle
	24	31	1/7	2B	pin12 should reserve 1u cap for ITE8512JX using
	25	19	1/7	2B	modify HDMI detect circuit to fix the monitor detection problem..
	26	55	1/7	2B	create EMI spring
	27	31	1/11	2B	per TXC report, we should change W1 cap to 18p
	28	41	1/11	2B	per IDT FAE suggestion, serial 22 ohm on DMIC_CLK can help DMIC performance
	29	37	1/11	2B	add 10u cap at JMB1, let 3.3V_ALE get lower drop voltage on MMB side.
	30	6, 19	1/11	2B	EMI demand add 33p cap on RGB signal.

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Title: X02 change list

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Model	Item	Page	Date	Rev.	Description
Pacino of Intel	1	45	10/08	B	Change screw holes define to meet ME request.

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